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16. ABSTRACT

This portion of the final report deals with dry processing - both etching and deposition - and present/future trends in semiconductor technology. In addition to a description of the basic apparatus, terminology, advantages, glow discharge phenomena, gas-surface chemistries, and key operational parameters for both dry etching and plasma deposition processes, a comprehensive survey of dry processing equipment (via vendor listing) is also included. In the semiconductor technology trends section of this report, the following topics are discussed: fine-line photolithography, low-temperature processing, packaging for dense VLSI die, the role of integrated optics, and VLSI and technology innovations.

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FORWARD

This report describes a portion of the work performed from July 1980 to March 1982 under Contract NAS8-33448 for the George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Marshall Space Flight Center, Alabama. The technical managers for MSFC were Mr. B. R. Hollis, Jr., Mr. R. F. Dehaye and Mr. J. M. Gould. This report was prepared by the Microelectronics Research Laboratory of the Department of Electrical Engineering, Mississippi State University, under the direction of the principal investigator Dr. Thomas E. Wade.

This final report has been divided into four areas of emphasis, with a separate comprehensive report for each area. These four areas represent the follwoing subject groupings:

PART I. Emphasis is on the realization of very dense metal interconnection for VLSI systems utilizing the lift-off process. Both a survey of lift-off techniques is presented as well as experimental and novel lift-off methods which have been investigated by the author.

PART II. Emphasis here is on multilevel metal interconnection system for VLSI systems utilizing polyimide as the interlayer dielectric material. A complete characterization of polyimide materials is presented as well as experimental methods

accomplished using a double level metal test pattern. A novel double exposure polyimide patterning process is also presented.

PART III. Emphasis is on dry plasma processing including a characterization of and an equipment survey for plasma etching, reactive ion etching, (reactive) ion milling and plasma depostion processes. Also included is an indication of future microelectronic trends, including patterning technology, lithography, materials deposition, packaging, etc.

PART IV. Emphasis here is on an evaluation of dielectric material for use in VLSI metal interconnection systems. A number of dielectric material types (or combination of materials) are experimentally evaluated using a second test pattern. Recommendations are presented based on these findings.

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I. DRY PROCESSING - AN OVERVIEW

Although many forms of dry processing have been used for integrated circuit manufacture for some time, the term "dry processing" has come to mean, principally, the use of gas and vacuum processes for the selective removal of material by etching or depositing desired thin films.

The processes employ ordinarily inert gases that are activated by an electric discharge, forming a plasma consisting of electrons, atomic and molecular ions, photons, and molecular fragments of radicals. These new species either react with materials to produce volatile products, which are then removed from the system, or react with other gases introduced to the system such that thin organic and/or inorganic films are deposited.

A. Dry Etching Processes

In the past, the density of integrated circuits as determined by their minimum linewidths has been limited to a great extent by available photolithographic techniques and equipment. With advances in photolithography such as wafer stepper projection systems and positive photoresists, the minimum dimension burden has shifted somewhat from defining the pattern to transferring it accurately to the film underlying the photoresist. Wet etching techniques have been used in the past to selectively attack unprotected areas of the film to be etched. While these techniques will continue to be used for films with linewidths greater than 5 μm, dry etching techniques and systems are being implemented to etch films with linewidths down to the submicron range.

With linewidths below 5 μm, wet etching techniques have at least two major shortcomings related to surface tension effects and isotropic etching characteristics. Surface tension effects are associated with the fluid flow of wet etchants in confined surface topologies, preventing the reaction products from freely exchanging. Reactive plasmas with the volatile reaction products they generate are not inhibited by smaller geometries.

The isotropic etch profiles associated with wet etching processes become important as the horizontal minimum linewidth approaches the vertical depth of the thin film to be etched. During an isotropic etch, the film is etched horizontally and vertically at the same rate, causing undercutting of the photoresist. The undercutting becomes significant as the ratio of the linewidth to film thickness approaches 5:1 [1]. With a typical aluminum film thickness of 1 μm, this translates to a minimum linewidth of 5 μm. Isotropic etching techniques cannot be used to etch 1 μm thick aluminum films with linewidths less than 4 μm.

One technique to achieve narrower linewidths is to reduce film thickness. A Japanese company is reportedly using aluminum films 0.5 μm thick. Etching is accomplished by continuously spraying the etchants over the wafer. Other manufacturers are reluctant to reduce aluminum thickness much below 1 μm because of the high electric fields produced within high density device structures. The optimum solution is to develop anistropic etching techniques which etch faster vertically than horizontally. Under the right conditions, dry etching techniques using reactive plasmas can provide anisotropic etch profiles required by high density devices.

1. Directionality in an Etching Process

The vast variety of structures, geometries and fabrication materials encountered in this technology imposes a wide range of requirements on the etching steps and often these requirements are very different for the various etch steps used in the production of a single device. The characteristic of etching processes which is becoming more and more important as the lateral dimensions of the lithography become small, is the so-called directionality of the etch process. This characteristic is defined in Figure 1 in which the lithographic pattern is in the x-y plane and the z direction is normal to this plane. If the etch rate in the x and y directions are equal to the etch rate in the z direction, the etch process is said to be isotropic or nondirectional and the shape of the sidewall of the etched feature is as shown in Figure 1. Etch processes which are anisotropic or directional have etch rates in z direction which are larger than the lateral (x or y) etch rates. The extreme case of directional etching in which the lateral etch rate is zero (to be referred to here as a vertical etch process) is also shown in Figure 1. It is not difficult to recognize why the directionality of an etch process is not a serious concern if the minimum lateral dimension in the lithography is very much larger than the thickness of the layer being etched. Conversely it is relatively easy to imagine situations in which the directionality of the etch process is crucial when the etch depth is comparable to the lateral dimensions involved and an example is shown in Figure 2. The situation is further complicated by the fact that in

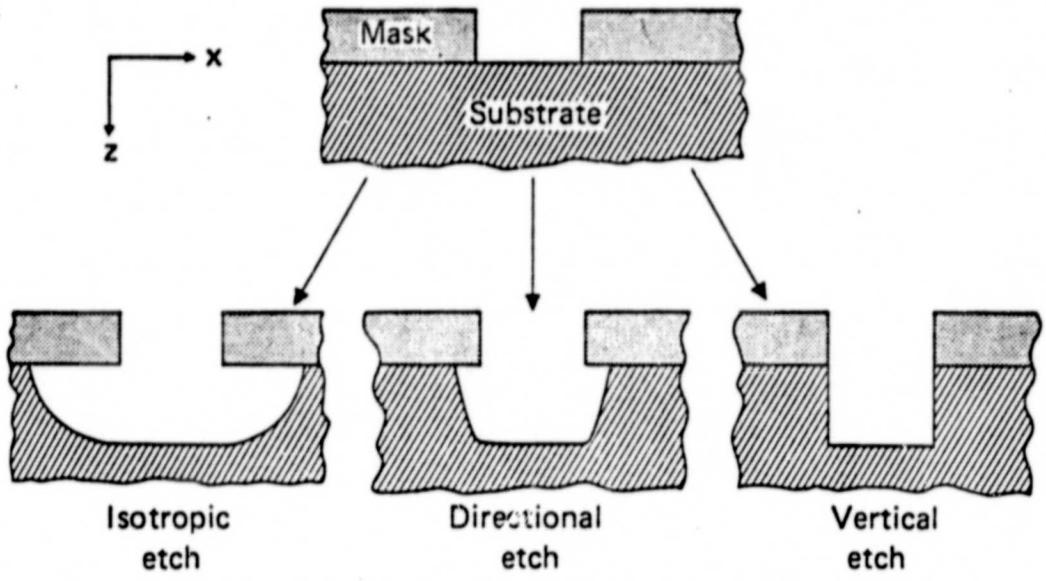


Figure 1. Directionality of etching processes

a large batch etching process, the etch rate is rarely uniform over all the wafers and therefore it is usually necessary to overetch to a certain extent to ensure completion of the etching on all of the wafers. The consequences of a 25% overetch on the example in Figure 2 are shown in the figure. The loss of dimensionality incurred by this overetching can be compensated for by making the initial lithography a little smaller (i.e., introducing a little "windage") but there are limits to the value of this approach.

Another consideration which will influence the desired shape of an etched profile is the difficulty associated with covering over very sharp sidewalls with a following deposition. Clearly, a tapered sidewall is easier to cover with line-of-site deposition methods but there are ways of depositing good continuous films over steps in the substrate topography [2,3]. The examples of Figure 1 and Figure 2 imply that vertical etch walls are always to

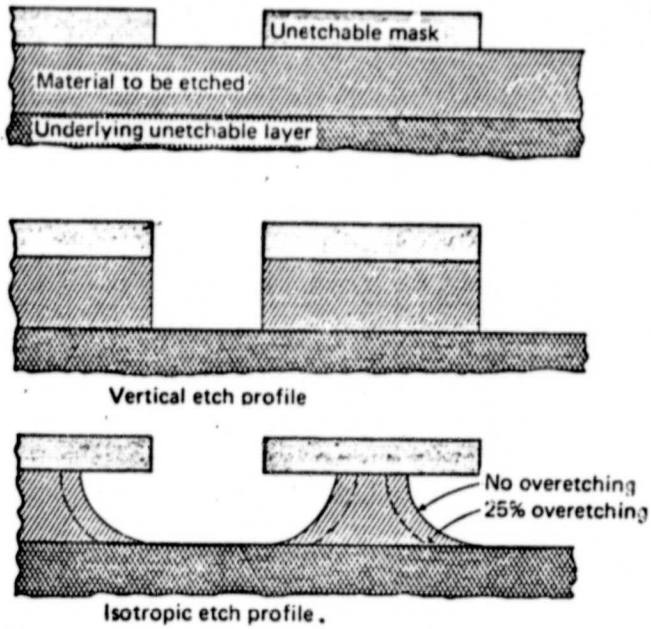


Figure 2. An example illustrating the loss of dimensionality incurred by isotropic etch processes when the etch depth is of the order of the lateral dimensions involved.

be preferred. There are situations, aside from the step-coverage problem just mentioned, in which an isotropic or partially isotropic etch process is preferable. An example of such a situation is shown in Figure 3. In this example an etching process which gives a perfectly vertical sidewall would require extensive overetching [4] to remove the material on the side of the step where as this material would be quickly removed with an isotropic etch process.

The shape of the sidewall of a feature etched with a vertical etch process can be manipulated to a certain extent by using erodable masks(i.e., masks which are removed by the etch process)

and introducing a taper on the sidewall of the mask during exposure and development.

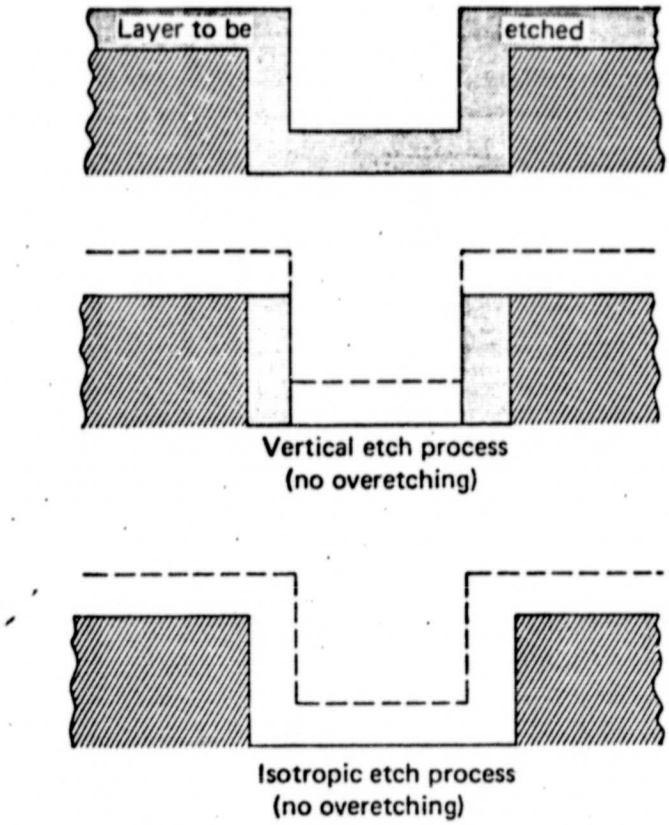


Figure 3. An example illustrating a situation where an isotropic etching process is perferable to a vertical etch process.

In summary, the shape of the sidewall of an etched feature is determined primarily by the directionality of the etch process and the optimum shape depends on many factors. However, the dimensionality problem depicted in Figure 2 is the main reason why the isotropic wet etch processes are being replaced by directional dry etching processes.

There are, of course, many other requirements of an etch process besides directionality which must be considered as well. These include etch rate, applicability to the materials involved, selectivity (ability to etch one material without etching another), cost, environmental impact, compatiblity with automation, cleaniness, etc.

As mentioned earlier, the basic concept of plasma etching is very straightforward. A glow discharge is used to generate chemically reactive species (atoms, radicals, ions) from a relatively inert molecular gas. The etching gas is chosen so as to produce species which react chemically with the material to be etched to form a reaction product which is volatile (at room temperature preferably). The etch product then spontaneously desorbs from the etched material into the gas phase where it is removed by the vacuum pumping systems. The key requirement is the volatility of the etch product. It is also important to recognize that rarely does the injected etch gas itself react with the surface being etched - the reactive species are formed by dissociating the relatively inert etch gas into reactive fragments. The most common example of the application of this concept is in the etching of carbonaceous materials in an oxygen plasma - a process referred to as plasma ashing [5] or plasma stripping. In this case the etching species are oxygen atoms and the volatile etch products are predominately CO, CO_2 and H_2O. In the late sixties this concept was extended to the etching of silicon and its compounds [6] in glow discharges of fluorine-containing gases

such as CF_4. In this case the volatile etch product is SiF_4 and the etching species are mainly fluorine atoms. In principle any material which reacts with fluorine atoms to form a volatile compound can be etched in this way (e.g., W, Ta, C, Ge, Ti, Mo, B, U, etc.). Chlorine-containing gases have also been used to etch some of the same materials but the most important used of chlorine-based gases has been in the etching of aluminum [7] which forms a volatile chloride but an involatile fluoride.

2. Advantages and Disadvantages of Plasma Etching

The major advantage of plasma etching is that it often can give highly directional etching. This is the major reason for current interest in this technology. Much discussion will be devoted to the directionality of the etch process later on. Other advantages relative to the wet etching process are lower chemical costs, reduced environmental impact, greater cleanliness and greater potential for production-line automation. The major disadvantages are the inability at present to etch certain materials which are important in particular technologies (e.g., Fe, Ni, Co), poor selectivity in some situations, high capital equipment costs, a tendency to cause radiation damage in some devices, and difficulty in process scale-up. This last disadvantage is a consequence of the complexity of the physical and chemical processes involved, combined with the large parameter space associated with the process. In spite of the serious nature of some of these problems, the inability of isotropic etching processes

to meet the demands of microstructure fabrication technology has forced the introduction of plasma etching into manufacturing environments.

3. Basic Apparatus, Terminology and Parameter

As was mentioned earlier, the first application of plasma etching was the removal of carbonaceous material in an oxygen glow discharge. The apparatus used for this plasma ashing process was usually very simple, consisting of a cylindrical dielectric vessel with an oxygen admission system at one end and a pump (often just a mechanical pump) at the other. The rf power was applied either by encircling the cylindrical vessel with an rf coil or by placing metal electrodes on opposite sides of the vessel as shown in Figure 4. The wafers to be etched are positioned in a rack of some kind in the center of the cylindrical vessel and usually no electrical connection is made to the wafers. This configuration is often referred to as a "barrel" system or a volume-loaded system. Naturally the availability of these "barrel" systems for plasma ashing applications led to their use in the plasma etching of silicon and other materials. The concern about the plasma radiation damaging sensitive devices led to the introduction of a cylindrical mesh to isolate the wafers from the energetic ions and electrons in the plasma. This protective mesh, often referred to as an "etch tunnel," [8] is included in Figure 4. Whereas silicon and its compounds can be easily etched in a "barrel" system, the etching tends to be isotropic. This is rarely a problem in plasma ashing applications but is a serious problem in certain etch steps in device fabrication as discussed previously.

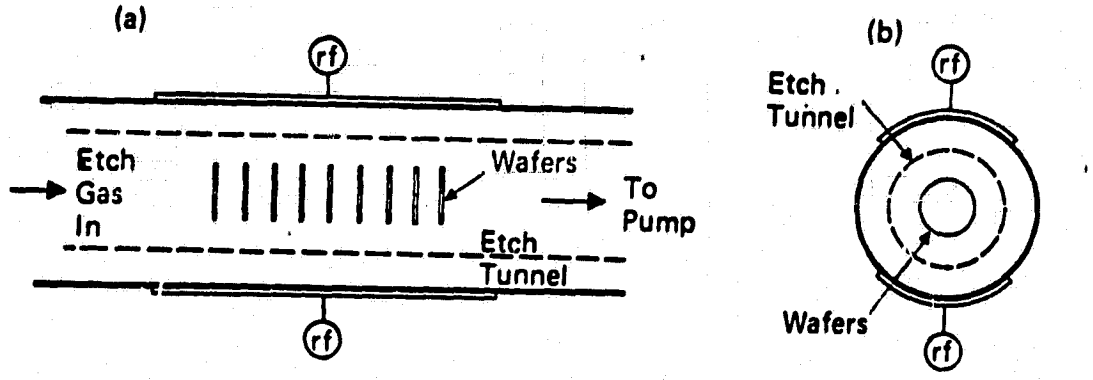


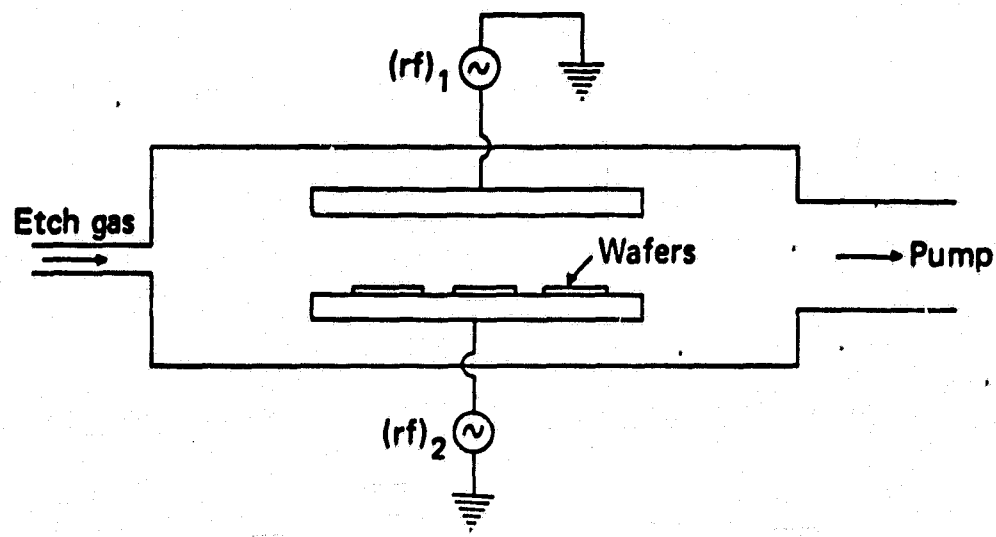
Figure 4. Barrel system with an etch tunnel.

The need for a directional etch process led to the use of a planar geometry very similar to the geometry used in rf sputtering technology. These planar systems are also called parallel plate systems or surface loaded systems. These systems have been used in two distinct ways: (1) The wafers are mounted on a grounded surface opposite the rf-powered electrode (cathode) or (2) the wafers are mounted on the rf-powered electrode (cathode) directly. This latter approach has been called "reactive ion etching" [9] or "reactive sputter etching." [10] Figure 5 is a schematic of a generalized planar etching system in which provision is made for applying rf power to either or both electrodes; a feature which is expected to provide valuable flexibility in planar etching systems. It has been demonstrated numerous times that planar etching systems are capable of highly directional, high resolution etching, and these successes suggest that the planar systems will become more popular in the future. Consequently the apparatus aspects of this discussion will be concerned primarily with planar systems. However,

the general concepts which will be covered are applicable to all types of etching systems.

Microwave plasmas are also being used in plasma etching, mainly in Japan. There are systems in which the wafer to be etched is immersed directly in a microwave plasma [11] and there are systems in which the wafer is placed downstream from the plasma [12]. In the latter configuration, the wafers are not subjected to energetic particle bombardment thus eliminating radiation damage concerns but this arrangement may cause problems in the etching of certain materials.

As is often the case with growing technologies, a rather complex terminology has been evolved to describe plasma etching processes. It is sometimes helpful to classify plasma etching or cleaning processes according to the nature of the discharge gas (inert or reactive), the volatility of the gas-surface reaction product and the electrical potential of the etched surface relative to the plasma potential. Most of the relevant plasma processes are classified in this way in Table 1 [13] and the following discussion will consider only situations in which a reactive gas is used and a volatile gas-surface reaction product is formed (i.e., plasma etching, plasma ashing, reactive ion etching or reactive sputter etching). Much of the following discussion will be restricted to the etching of silicon and its compounds by flourine containing gases primarily because this system is technologically important and it is more thoroughly understood than other chemical systems.



$(rf)_1 \neq 0$ $(rf)_2 = 0$ — Plasma etching
$(rf)_1 = 0$ $(rf)_2 \neq 0$ — Reactive ion etching
$(rf)_1 \neq 0$ $(rf)_2 \neq 0$ — Triode etching

Figure 5. Generalized planar etching system.

One of the major obstacles to the routine implementation of plasma etching is the extensive parameter space associated with the process. These parameters can be categorized to a certain extent as shown in Figure 6 [14] but the complexity is such that it does not seem possible at present to specify a particular etching process well enough that the process can be routinely scaled-up and implemented in various systems. An example of a process which is easily specified is ion implantation - the nature of the ionic species, the energy and the dose per unit area completely specify the process.

TABLE 1

CLASSIFICATION OF PLASMA PROCESSES

Type of Discharge / Extent of Ion Bombardment	Inert Gas Discharge	Reactive Gas Discharge	
		Involatile Gas-Surface Product	Volatile Gas-Surface Product
Minimal (Sample on Ground Plane)	Plasma Cleaning	Plasma Anodization (Oxygen plasma)	Plasma Etching Plasma Ashing (oxygen plasma)
Extensive (Sample on Target Electrode)	Sputter Etching	Reactive Sputter Etching	Reactive Sputter Etching Reactive Ion Etching

Although the overall parameter problem is formidable in plasma etching, there are some procedures which can eliminate some of the difficulties. For example, the various parameters associated with the discharge gas are related to one another and can be handled reasonably systematically. The parameters in question are the pressure in the etching chamber P, the flow rate of the etching gas Q, the effective pumping speed at the etching chamber S, the mean residence time for etch gas molecules in the etching chamber τ and the volume of the etch chamber V. Figure 7 is a schematic diagram of the vacuum and gas flow-related aspects of an etching system showing these parameters. The associated instrumentation and control which should be part of any etching system consists of: (a) a flow meter to measure Q, (b) a pressure gauge to measure P, (c) a leak valve to control Q and (d) a variable conductance between the pump

and the etch chamber to enable P and Q to be controlled independently. With these features, the gas flow rate can be established initially and then the pressure can be set by adjusting the pump-etch chamber conductance. These parameters associated with the discharge gas are related to each other by Q=SP and τ=V/S. It is important to recognize that the pressure in the etch chamber can be adjusted in either of two ways: (1) Keep Q constant and vary S (i.e., vary τ) or (2) Keep S constant (i.e., τ) and vary Q. This latter procedure is accomplished by keeping the ratio of Q/P constant. It is not clear which of these two methods of changing pressure is to be

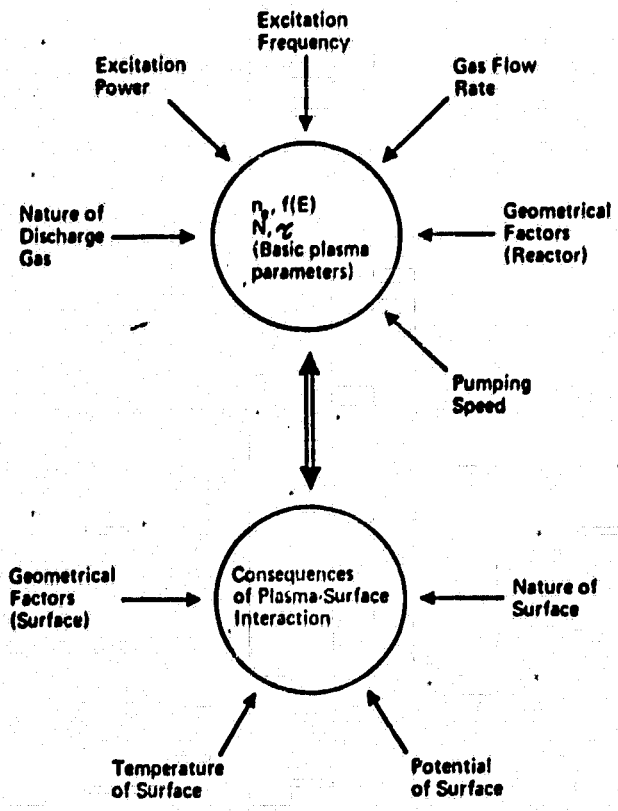


Figure 6. Representation of the parameter problem in plasma etching systems. n_e - electron density, f(E) - electron energy distribution function, N - gas density, τ - residence time for gas molecules in plasma system.

preferred but the fact that in plasma etching some of the etch gas is consumed by the process may be an argument in favor of the constant Q approach. That is, when S is kept constant, at very low flow rates

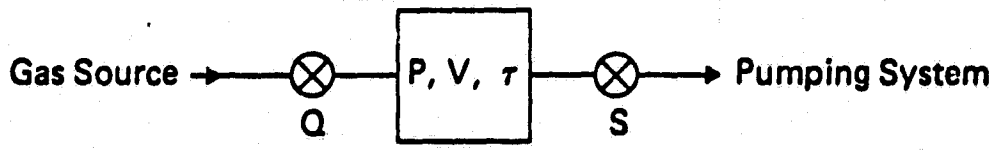


Figure 7. Vacuum schematic of plasma system. Q - etch gas flow rate, P - pressure in etching system, V - volume of etching system, τ - residence time for gas molecules in plasma system, S - pumping speed at etching system.

the etching may consume a major fraction of the etching gas and this will mean the dominant gas in the system is no longer the etch gas but the etch product. Keeping Q constant reduces this difficulty but introduces the complication that the residence time τ is not kept constant. The pressure dependence of an etch rate, for example, can be very different depending on which pressure variation procedure is followed.

4. The Reactive Gas Glow Discharge

It is useful to consider briefly the types of particles that are present in a reactive gas glow discharge and to estimate the densities of these particles. A CF_4 glow discharge will be used for illustration purposes. Prior to the initiation of the glow discharge the only species present, of course, are CF_4 molecules. The density of CF_4 molecules depends on the operating pressure which ranges from about 1 Pascal (7.52 millitorr) to about 150 Pascals (1.13 Torr). This corresponds to a gas density ranging from

2.7×10^{14} to 4×10^{16} molecules per cm^3. The mean free path between collisions at these gas densities depends somewhat on what species are involved but an estimate might be about 6000μm at the low pressure end to about 40μm at the high pressure end. These dimensions even at the high pressure end are larger than the amplitude of most topographical detail generated by the etching processes. That is to say, the neutral species are incident on surfaces from all directions but, on the average, make their last gas phase collision well above the surface relative to the depth of etched features. When the glow discharge is established, often a large percentage of the CF_4 molecules are dissociated and the CF_4 partial pressure will decrease [15]. The rate at which CF_4 molecules are dissociated is difficult to estimate. An order of magnitude guess can be derived from estimating the current of ions striking the cathode [16] (powered electrode) and this leads to $1\text{-}10 \times 10^{15}$A CF_4 molecules dissociated per second where A is the cathode area in cm^2. For a 20cm diameter cathode electrode this becomes $\sim 10^{18}$ CF_4 molecules/sec dissociated. Typical CF_4 gas flow rates range from a few standard cm^3/min (sccm) to several hundred sccm (1 sccm = 4.48×10^{17} molecules/sec). It is desirable to have the CF_4 gas flow rate much larger than the dissociation rate of the glow discharge and thus it can be seen why flow rates of at least 10 sccm are desirable in a moderate size plasma etching system.

A glow discharge [17] is a self-sustaining type of plasma. In a dc glow discharge electrons are created by the impact of positive ions colliding with the cathode electrode. These electrons are

accelerated back into the glow discharge and collide with and ionize molecules. Some of the positive ions so formed are accelerated back toward the cathode and so on. In dc glow discharges the electrons can gain energy only from the strong electric field in front of the cathode. However, in rf glow discharges electrons can acquire energy from various time-varying fields at almost any plasma-surface boundary or even in the bulk plasma, as well as from the cathode electric field. Consequently, rf discharges can be operated at lower pressures than dc discharges. The glow discharge contains approximately equal numbers of positively charged particles (positive ions) and negatively charged particles (electrons and negative ions). The density of charged particles in the types of glow discharges used for plasma etching depends strongly on the system parameters but usually will be in range of 10^9 to 10^{11} charged particles per cm^3. The degree of ionization (i.e., ion-neutral ratio) is probably in the range 10^{-4} to 10^{-6}.

In CF_4 discharges, the most abundant positive ion is CF_3^+ which is formed most often by $e_4+CF_4 \rightarrow CF_3^+ + F + 2e$. This is the most probable ionization process for CF_4. (The ion CF_4^+ is found only in high pressure situations [18]). Many other processes are possible which produce other ions such as F^+, F^-, CF_2^+, CF^+, C^+ and these ions all can be found in a CF_4 glow discharge. However, the concentrations of these other ions will be significantly less than that of CF_3^+ not only because they have a smaller probability of being formed but also because many of these ions are consumed in reaction with CF_4 (e.g., $CF_2^+ + CF_4 \rightarrow CF_3^+ + CF_3$) whereas CF^+ does not react with CF_4. An

example of a mass spectrum of positive ions extracted from a CF_4 glow discharge is shown in Fig. 8 [13]. Very little information is available on the concentrations and types of negative ions in such a glow discharge. However, the concentration of negative ions is substantially less than the concentration of positive ions because of the charge neutrality requirement for the glow discharge (i.e., density of electrons + density of negative ions = density of positive ions).

In addition to neutral CF_4 molecules, electrons, positive ions and negative ions, there is a large concentration of radicals, the most abundant being F atoms and CF_3 radicals. The process which is responsible for most of these species is $e+CF_4 \rightarrow CF_3+F+e$ and it can be expected that this reaction is more common in a CF_4 discharge [16] than the ionization process discussed earlier producing CF_3^+ and F. Since these radicals are probably produced at a faster rate than positive ions, and unlike ions, radicals can survive collisions with surfaces in the etching system, one would expect radicals to exist at concentration levels substantially larger than ionic concentrations. Relatively few absolute measurements of radical concentrations have been made but in one instance the F atom pressure was found to be about 20 percent of the total gas pressure in the etching system [19]. It is not clear that this is a typical result but it is clear that the F atom pressure will be very dependent on the many parameters of the experimental system. Other radicals such as CF_2, CF and C as well as larger species such as C_2F_5 are most probably present in the discharge but at lower concentrations.

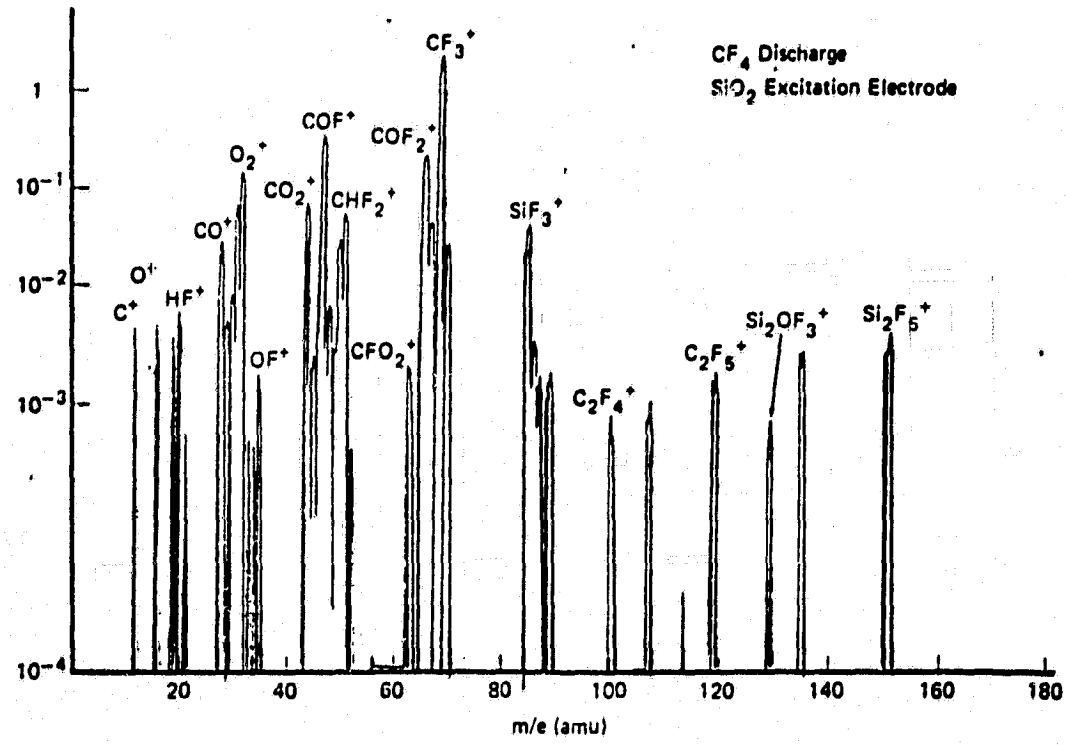


Figure 8. Mass spectrum of positive ions extracted from a CF_4 glow discharge with a SiO_2 excitation electrode. (See ref. 13)

5. Potential Distribution in a Planar System

It is often very useful to have a knowledge of the potential distribution in glow discharge systems. In plasma etching this is particularly true because the energy with which particles are incident upon the etched surface is a very important factor in determining the etching behavior. The discharges used in this technology are usually obstructed; that is the anode is sufficiently close to the cathode to eliminate the positive column. The discharge consists of the cathode dark space and a negative glow. The approximate potential distribution between a negatively biased cathode and a grounded anode for a dc discharge is shown in Fig. 9. The applied

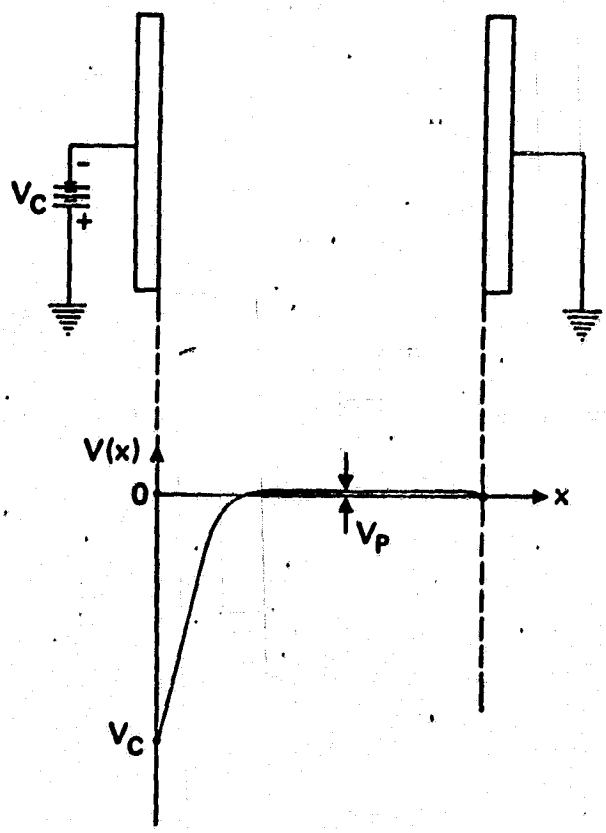


Figure 9. Approximate potential versus distance plot for an obstructed dc glow discharge.

voltage appears across the cathode dark space, whereas the negative glow region has little or not electric field and has a potential very close to that of the grounded anode. This is true for most gases. In the rf discharges used in plasma etching, the situation is similar and the time average potential is shown in Fig. 10. The basic difference between this time-averaged rf potential and the dc situation is that the potential of the negative glow region, to be referred to as the plasma potential V_p, is significantly positive with respect to the grounded anode. The magnitude of the plasma potential in a planar system depends on many things, some of which will be discussed shortly. The instantaneous value of

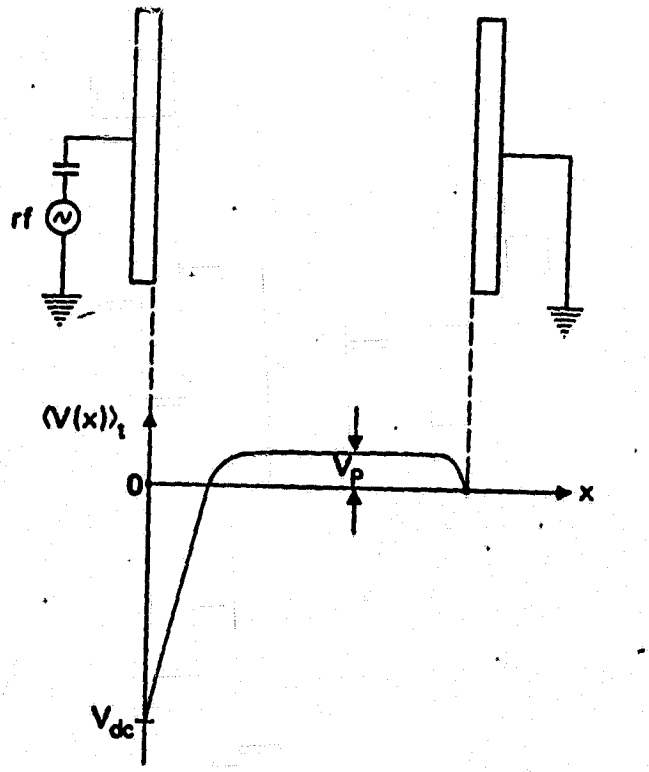


Figure 10. Approximate time-averaged potential versus distance plot for a capacitively coupled planar rf glow discharge system with wall area much greater than cathode electrode area.

the plasma potential and of the potential of the cathode electrode are shown in Fig. 11. The time-average of the plasma potential V_p, the time-average of the cathode potential V_{dc} and the peak-to-peak rf voltage applied to the cathode are related approximately as shown in Fig. 11. An important fact to remember is that the plasma potential V_p is usually as positive or more positive than the potential of any electrode in contact with the plasma. This is a result of the large mobility electrons - electrons tend to rush towards a positively biased electrode thus depleting the glow discharge of negative charge carriers and causing the plasma potential

to increase. Electrons can respond to the rapidly varying rf potentials whereas most ions respond only to the time-averaged potential as shown in Fig. 10. For this reason it is recommended that the dc potential of the cathode electrode be measured whenever possible and used as a control parameter in preference to rf power. In addition, a measurement of V_{dc} along with a measurement of the peak-to-peak applied rf voltage can be used to estimate V_p as shown earlier in Fig. 11.

$$2V_p \sim \frac{(V_{rf})_{pp}}{2} - |V_{dc}|$$

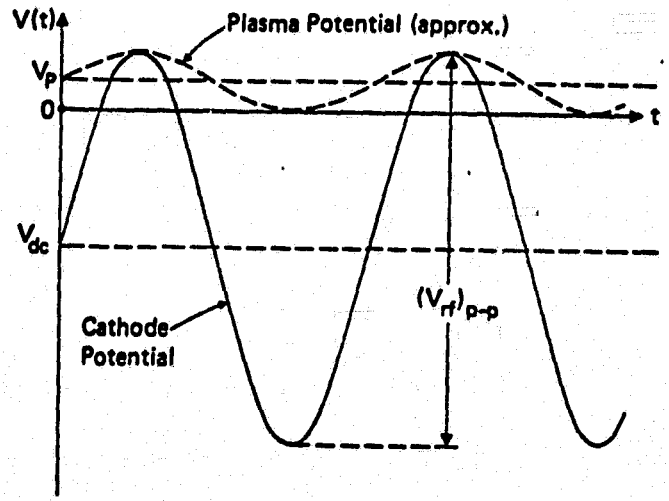


Figure 11. Approximate cathode and plasma potential waveforms. V_p - plasma potential, V_{dc} - self-bias voltage on cathode electrode, $(V_{rf})_{p-p}$ - peak-to-peak rf voltage applied to cathode.

There are several factors which can cause the plasma potential V_p to be well above ground potential. An approximate electrical equivalent circuit of a typical rf planar discharge system is shown in Fig. 12 [20, 21]. The capacitances represent the capacitive nature of the discharge-surface boundaries or sheaths and the diodes represent the high mobility of plasma electrons. It follows from this equivalent circuit that the plasma potential V_p is determined by the relative magnitudes of the sheath capacitances (i.e., by capacitive voltage division) which in turn depend primarily on the relative areas of the cathode electrode and other surfaces in contact with the discharge. If the system is perfectly symmetric (area of cathode equals area of grounded surfaces) the plasma potential will be very large and both the cathode and the grounded surfaces will be subjected to energetic ion bombardment to approximately the same extent. This situation is believed to exist in certain types of plasma etching systems in which large plasma potentials have been measured [22]. If the area of the cathode electrode is significantly smaller than the area of other surfaces in contact with the discharge, the plasma potential will usually be small (~20 to 50 volts positive with respect to the grounded vacuum chamber).

A second factor which can cause a large plasma potential is the presence of a positively biased surface in contact with the discharge. This effect is shown in Fig. 13 [21] in which it can be seen that the plasma potential V_p is unaffected by negative voltages applied to an electrode in the plasma but increases rapidly when the applied voltage is positive. It is not often that positive voltages are applied to

surfaces in glow discharges but great caution is recommended in the interpretation of phenomena resulting from such an exercise.

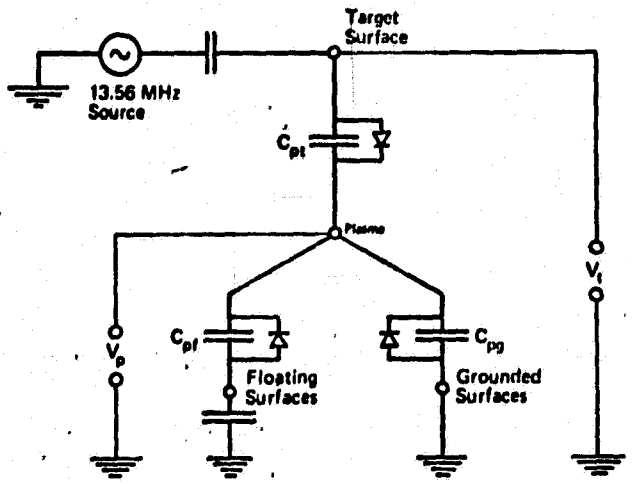


Figure 12. Approximate equivalent circuit of rf planar discharge system. (See References 20 and 21.)

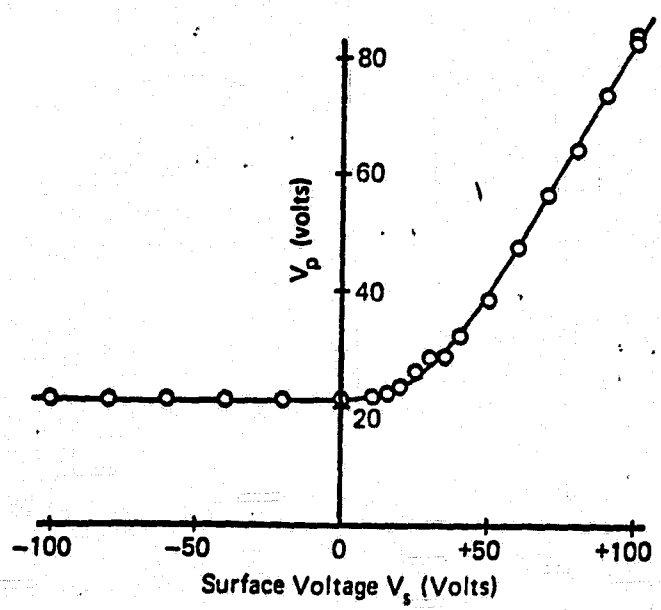


Figure 13. Plasma potential V_p as influenced by a voltage V_b applied to an electrode in contact with the discharge. (Data from Reference 21.)

A third cause of a large plasma potential is a dc grounded excitation electrode. If the electrode is made of an electrically conducting material which is connected directly to a rf generator or if there is some other low impedance dc path to the ground, the electrode surface is forced positive by the applied rf voltage (i.e., there is no opportunity for a dc self-bias to develop). Since the plasma will follow positively biased surfaces, the plasma potential will be similar to the half-wave-rectified applied rf voltage.

6. Gas-Surface Chemistry

Some experiments on the etching of silicon and silicon compounds with xenon diflouride, without a plasma, both provide a means for etching a pattern in silicon compounds without using a photo-resist mask [23] and add further understanding to the etching of these materials [24]. XeF_2 is essentially a source of fluorine atoms, and it is found that xenon difluoride etches silicon at room temperature without radiation or any other external energy input, with a reaction probability ~ 10^{-2} (Fig. 14). Silicon oxide, and several other compounds, are not etched under these circumstances, but etching does proceed if the oxide sample is simultaneously

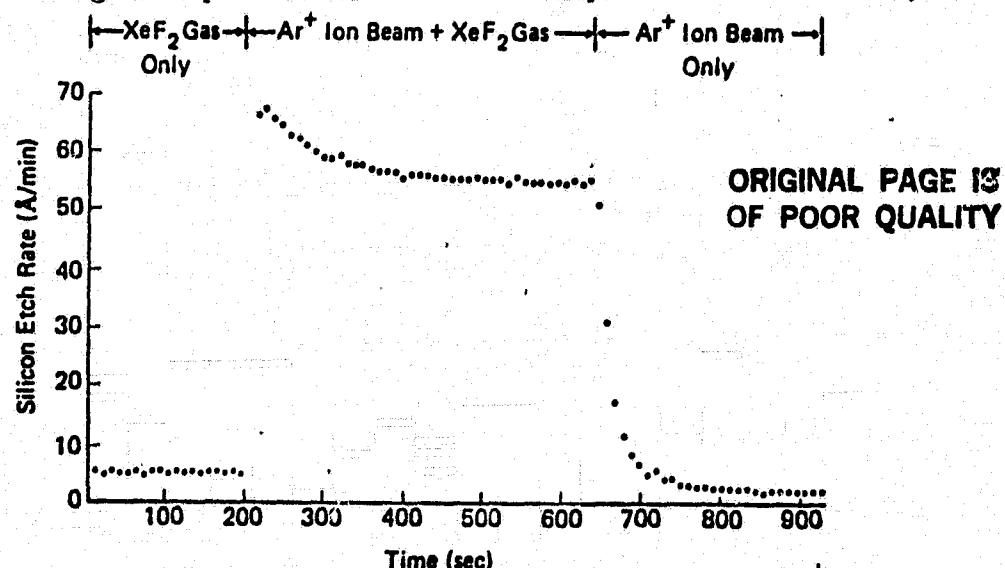


Figure 14. Ion-assisted gas-surface chemistry using Ar^+ and XeF_2 on silicon.

exposed to a beam of electrons or ions (Fig. 15). The etch rate of Si is also enhanced by electrons or ions (Fig. 14). It had earlier been found that silicon is similarly etched by molecular fluorine without a plasma, but only with a very low reaction probability ($\sim 10^{-6}$); silicon oxide was not etched by fluorine until exposed to short wavelength light, which also enhanced the silicon etch rate. This gives a clear example of how effective a plasma can be in creating chemically active species, with the implication in this example that fluorine, already very reactive by most standards, can have its reactivity enhanced by four orders of magnitude by plasma dissociation.

The experiments using XeF_2 seem to confirm a mechanism for etching of silicon and silicon oxide implied in some earlier results: if one removed silicon oxide from ion bombardment, e.g., by moving it from target to counter-electrode in reactive ion etching, its etch rate dropped precipitously, while the etch rate of silicon was much less affected. In addition, oxide was always etched directionally, but silicon could sometimes be undercut. The inference made [24] is that oxide etches only with the assistance of ion bombardment, while silicon has both a purely chemical and an ion-assisted component.

Results obtained in a triode plasma etcher [25], where the energy of ion bombardment can be continuously varied, tend to confirm the above model for silicon. But grounded oxide is etched in this system, in contrast to other reactive ion etch results. It could be argued that the low pressures (10-30μm) used in the

triode encouraged fast secondary electron bombardment from the target onto the wafer, or that the plasma potential was unusually high. However, one also needs to explain how oxide can be etched rapidly in a barrel reactor even inside an etch tunnel where ion bombardment is minimal [26]. The oxide etch rate does increase with reactor temperature, and temperatures do frequently exceed 200°C in such systems. This suggests that the silicon oxide-fluorine reaction can also be activated by heating as well as by bombardment, and this is not surprising. But this does not explain why, in such reactors, the initial or "cold" etch rate is a significant fraction of the final "hot" rate; the reactive ion etch results suggest a zero etch rate under these circumstances. Further

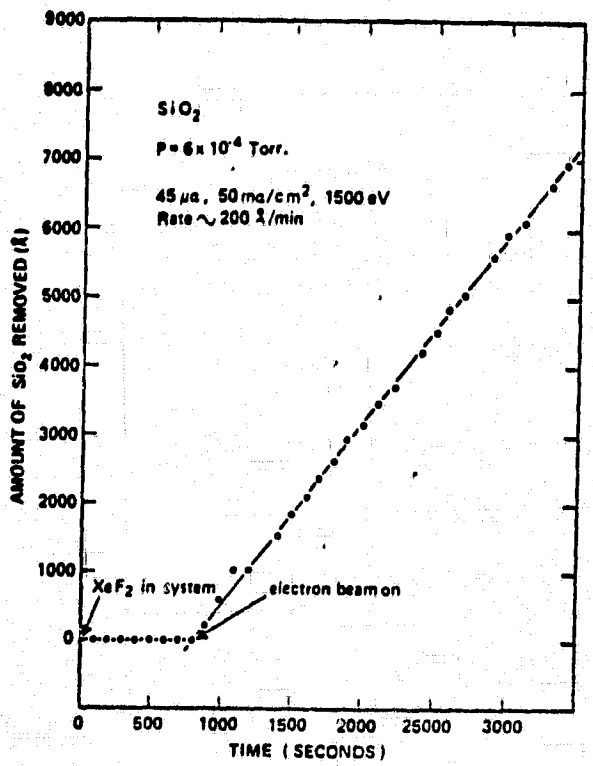


Figure 15. Electron-assisted Gas-surface Chemistry using 1500 eV electrons and XeF_2 on Si_3N_4. P(total) = 6 x 10^{-4} Torr with most of the ambient gas being xenon. Neither exposure to XeF_2 nor an electron beam produces etching by itself. Simultaneous exposure produces an etch rate of ~600 Å/min.

evidence that silicon oxide can be etched other than with ion-assistance is the recent observation [27] that quartz can be etched by CF_3 radicals, again without heating, downstream from a discharge source of these radicals. So it seems that a great deal of progress has been made with the surface studies approach to understanding the etching mechanisms of silicon and silicon oxide, but that some further refinements are required.

7. Flow Effects

Although the basic interaction at the surface is of prime importance, one must not lose sight of other requirements such as etch rate uniformity and repeatability. It is also easy for someone with a physical sputtering background to forget that the etching gas is consumed, and the fraction of CF_4 converted to SiF_4

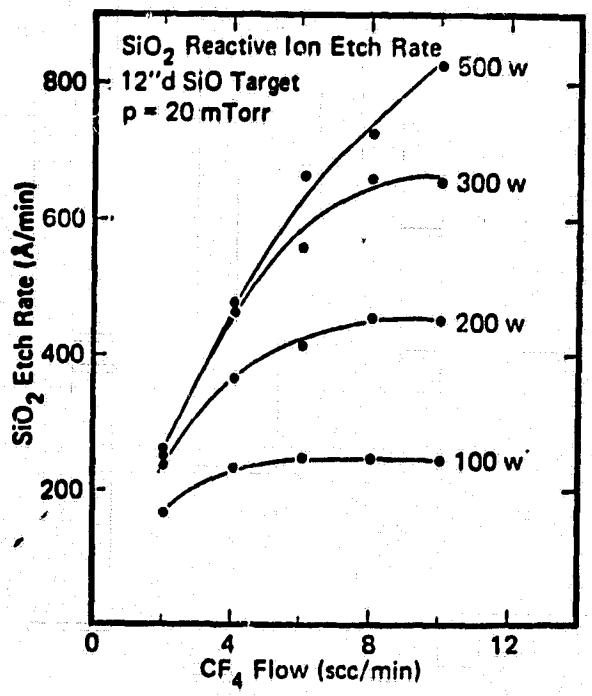


Figure 16. Variation of etch rate of sputtered quartz with flow rate of CF_4 for various power inputs.

can become large enough to give rise to a flow rate effect [28] (Fig. 16). By using a simple mass balance approach, one can predict a maximum achievable etch rate - the 100% utilization case in Fig. 17 - and it is surprising how efficient the plasma etching can be under such circumstances. It is also surprising how frequently flow rates influence the etching process, albeit often in unobvious ways; for example, the apparently quite different etch rate vs. power behaviors shown in Fig. 18 are really due to a flow effect. High

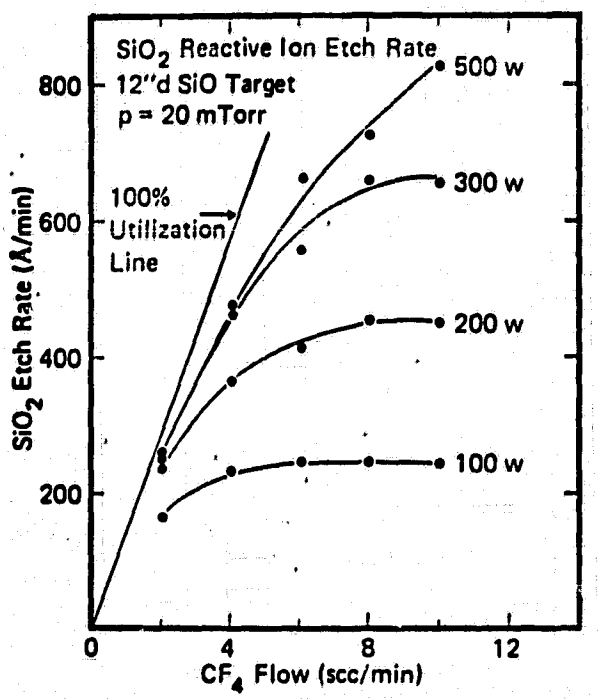


Figure 17. Showing the 100% utilization line, for complete conversion of CF_4 to SiF_4.

utilization rate effects tend to affect mostly plasma and RIE systems. Higher pressure barrel planar diode reactors have much higher pumping speeds and as a result, active species can be pumped away before they react with the wafer (Fig. 19) [28].

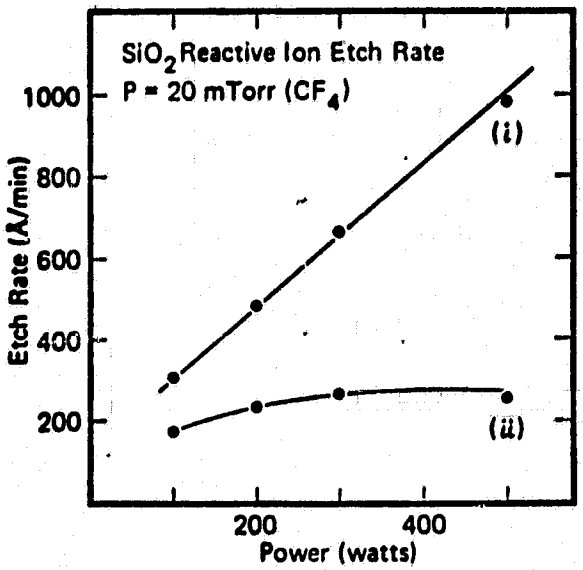


Figure 18. Etch rates of SiO_2 as a function of input power: (i) at 20 sccm CF_4, and (ii) at 2 sccm CF_4.

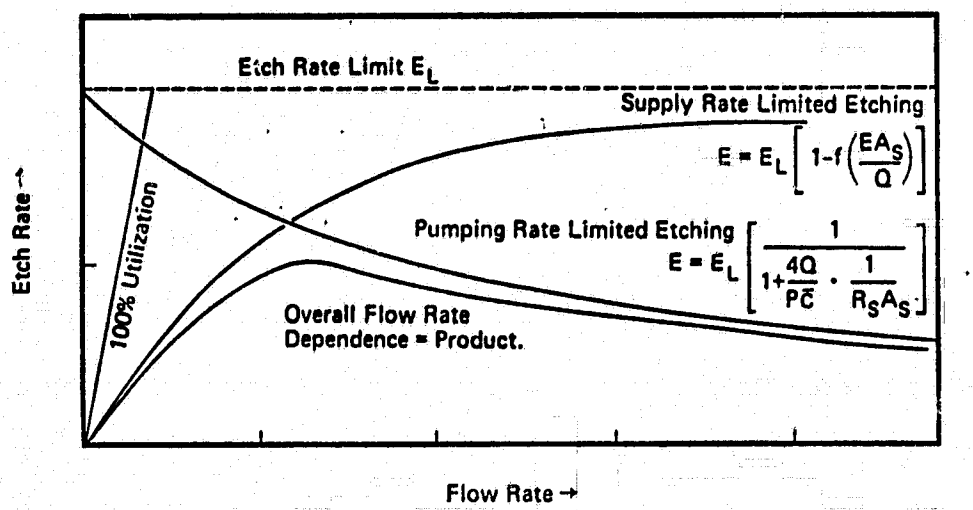


Figure 19. Theoretical etch rate versus flow rate for the flow-rate-limited and pumping-speed-limited cases, and their product -- the generalized flow rate dependence. (Ref. 28)

8. Glow Discharge Processes

In this discussion of plasma etching, the etching of silicon and its compounds in fluorocarbon glow discharges will be used as an illustrative example. The reasons for this choice are both the technological importance of this materials system and the fact that most of the basic studies of plasma etching have been performed on the silicon-fluorine system. It is hoped that the concepts which have evolved from those studies can be cautiously extended to other materials combinations. However, there are some characteristics of the silicon-fluorocarbon system which are not shared by other systems and which might influence the plasma etching behavior. These characteristics include: (a) the fact that CF_4 (and other small saturated fluorocarbons) does not chemisorb on silicon or its compounds [29]; (b) fluorine atoms react spontaneously with silicon at room temperature to form SiF_4; (c) silicon can abstract fluorine from carbon. It is difficult to assess the importance of these characteristics on the etching behavior at this time but it is to be expected that systems which behave differently in the above respects will also behave differently in a plasma etching environment.

a. Additive Gases in the CF_4 Plasma Etching of Silicon and Its Compounds

a.1 Gases which combine with carbon

One of the first gases added to CF_4 glow discharges was oxygen [30] and it has been consistently observed [11, 12, 19, 31-34] that the etch rate of silicon increases as small concentrations

of oxygen are added to fluorocarbon glow discharges. It has also been observed that the density of fluorine atoms [19, 32] (as measured by optical emission spectroscopy) increases as oxygen is added to fluorocarbon glow discharges. An example of both the etch rate dependence and the dependence of the F atom optical emission intensity on the percentage of oxygen in a CF_4 discharge is shown in Fig. 20 [19].

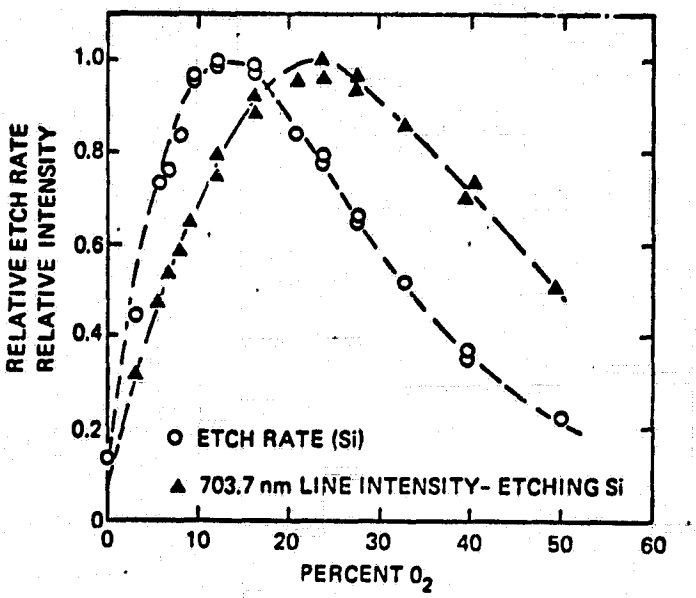


Figure 20. The normalized etch rate for Si and the normalized intensity of the emission from electronically excited F atoms (703.7 nm line) versus the O_2 concentration in the CF_4-O_2 etch gas (data from ref. 19).

The detailed mechanisms through which the addition of oxygen leads to an increased density of fluorine atoms and consequently an increased silicon etch rate, have been the subject of considerable discussion and study. Independent studies have shown that CF_4 molecules do not react with oxygen atoms [35, 36] or molecules. Furthermore, the addition of oxygen is not expected to increase the density or energy of electrons in the plasma; in fact, a decrease in

the F atom excitation probability has been measured [19]. Thus the enhanced F atom density caused by oxygen addition cannot be due to an increase in the dissociation rate of CF_4. Therefore the reactions responsible must be between oxygen atoms or molecules and the radicals formed by the dissociation of CF_4. This much is certain; beyond this, various possibilities must be considered [33]. Consider first of all, the gas phase oxidation of CF_3 by oxygen atoms presumably to form CO and three F atoms eventually. CF_3 by itself cannot etch silicon as was mentioned earlier but the gas phase oxidation process has formed three F atoms, which can etch silicon, and one relatively unreactive CO molecule. Suppose the CF_3 radical reaches the Si surface to form one adsorbed C atom and three adsorbed F atoms. An oxygen atom can now react with the adsorbed carbon and the fluorine atoms are available for etching. The consequences of this surface process are difficult to distinguish from the gas phase process. Furthermore, the surface reaction need not occur on the etched surface to be effective. Suppose a CF_3 radical adsorbs on a wall in such a way that either a F atom or an O atom can react with it. If the F atom arrives first the CF_3 and the F recombine to form CF_4 and thus one F atom has been lost for etching. If, however, the O atom arrives first and reacts with the CF_3 to form CO and three F atoms, three F atoms have been made available - a net gain of four F atoms when one includes the one lost above.

A more general point of view is to consider the consequences of forming CO or CO_2 by whatever process one chooses. The carbon

entered the etching system as a CF_4 molecule and is leaving as CO or CO_2 [16]. Thus four F atoms have been made available for etching.

Most plasma etching studies of the role of oxygen have involved the addition of molecular oxygen. However, similar effects can be obtained either by using oxygen-containing fluorocarbons such as COF_2 or CF_3OOCF_3 [34] or by adding oxygen-containing gases such as CO_2 to CF_4. Nitrogen atoms form strong chemical bonds to carbon and hence nitrogen additions might be expected to increase the F atom density also. However, the information available at present indicates that nitrogen is relatively ineffective in this role [34].

a.2 Gases which combine with fluorine

Molecular hydrogen is known to react with fluorine to form HF and as expected the addition of hydrogen to a CF_4 plasma decreases the F atom-concentration dramatically. The etch rate of silicon also decreases as would be expected and this is not in itself a useful result. However, it was found that the etch rate of SiO_2 decreased much more slowly than the etch rate of Si as hydrogen was added to a CF_4 plasma [37]. This increase in the etch-rate ratio of SiO_2-to-Si is very useful in those etching applications where a thin layer of SiO_2 must be etched down to an underlying layer of Si without etching into the Si appreciably. Figure 21 [38] shows the magnitude of this effect in a reactive ion etching system and it is expected that this approach will be used extensively to manipulate SiO_2-to-Si etch-rate ratios in plasma etching technology.

Other gases which tend to consume F atoms will also increase the SiO_2-to-Si etch-rate ratio. Gases which have been studied include C_2F_4 [34], C_2H_4 [39], C_2H_2 [40], CHF_3 [10], H_2O as well as the larger saturated perfluoroalkanes.

a.3 SiO_2-to-Si etch rate selectivity mechanism

The mechanism responsible for the increase in the SiO_2-to-Si etch-rate ratio involves a combination of two processes discussed previously - the deposition of an involatile residue (i.e., carbon) and the role of oxygen. There are several ways in which carbon can be deposited on surfaces in fluorocarbon discharges. One way is the dissociative chemisorption of CF_3 or other fluorocarbon radicals [29]. A second way is bombardment of the surface with CF_3^+ or other fluorocarbon ions [41]. Figure 22 [41] shows (a) an Auger spectrum of a silicon surface cleaned with 500eV Ar^+ bombardment and (b) an Auger spectrum of the same surface following bombardment with CF_3^+ ions (500eV, 5×10^{16} ions/cm^2). Note that the

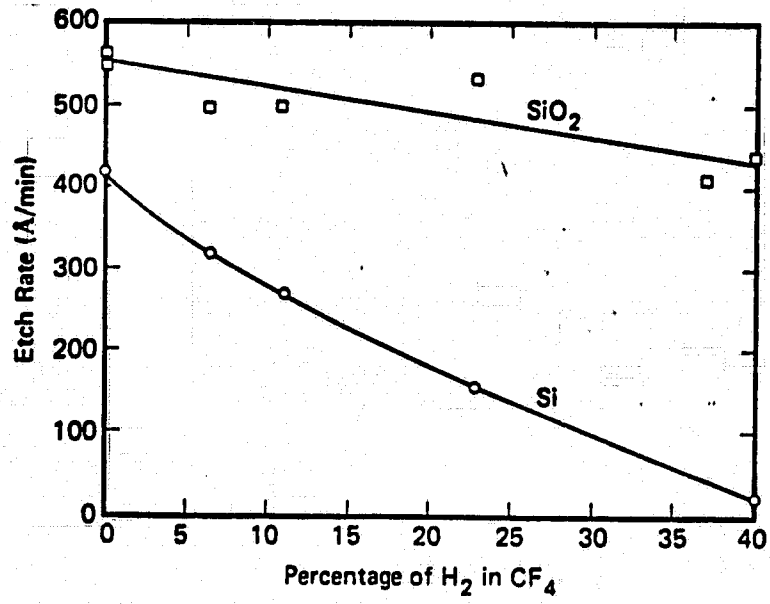


Figure 21. The etch rate of Si and SiO_2 (measured in a reactive ion etching configuration) as a function of the concentration of H_2 in the CF_4-H_2 etch gas.

CF_3^+-bombarded surface is completely covered with carbon. These spectra were recorded in an ultrahigh vacuum system using ion beams and there were no gas phase F atoms present. In a plasma etching system, surfaces are subjected to carbon deposition as well except that in a pure CF_4 plasma, there are enough fluorine atoms to remove the deposited carbon by re-forming CF_4. However, as gases which react with fluorine are added, the carbon deposition tends to consume a higher and higher fraction of the fluorine atoms which arrive at the surface and the etch rate decreases. This argument applies to all surfaces and the selectivity is attributed to the oxygen in the SiO_2 lattice which is able to assist in the removal of the adsorbed carbon by forming volatile CO or CO_2. As the discharge is made more and more fluorine deficient by the addition of a gas which reacts with fluorine, the carbon accumulation becomes more severe on the Si surface until all the incident fluorine reacts with

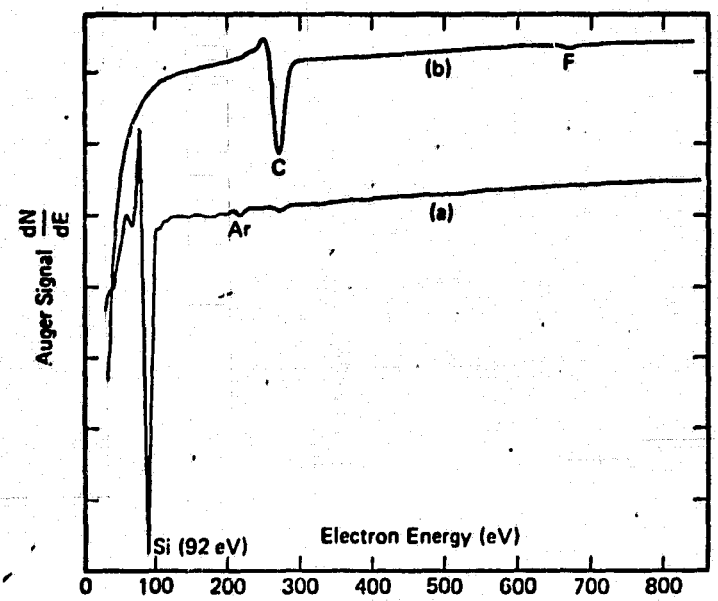


Figure 22. Auger electron spectrum from (a) Si surface cleaned by 500 eV Ar^+ ion bombardment and (b) same surface as (a) after bombardment with 5 x 10^{16} CF_3^+ ions/cm^2 (500 eV). Experiments were performed in an ultra-high vacuum system using an ion beam which was not mass analyzed.

the adsorbed carbon and the Si etch rate drops to zero. At the same time some of the adsorbed carbon reacts with the oxygen in the SiO_2 lattice thus leaving some F atoms available to etch the Si component of the SiO_2. This mechanism is supported by some Auger spectroscopy studies [42] carried out in a plasma etching system (after the etching was completed and the etch gas pumped out). Auger spectra were recorded of Si and SiO_2 surfaces simultaneously exposed to CF_4-H_2 discharges and the relative intensities of both the Si and the C Auger peaks are plotted versus the hydrogen concentration in the CF_4 etch gas in Fig. 23 [42]. More carbon deposition can be seen on the Si surface relative to the SiO_2 surface as hydrogen is added and silicon is no longer observable on the Si surface when it is easily observable on the SiO_2 surface.

The fact that SiO_2 continues to be etched under conditions where Si etching has stopped has been interpreted as indicating F atoms etch Si but CF_3 radicals etch SiO_2. This statement is probably correct but it is not complete. Fluorine atoms certainly are responsible for the etching of Si but fluorine atoms will also etch SiO_2 very rapidly in the presence of energetic radiation. CF_3 radicals incident on Si cause no etching but not because CF_3 radicals do not react with Si (they do [29]) but because the carbon blocks the etching process. CF_3 radicals on SiO_2 can contribute fluorine to the etching process because the carbon combines with the oxygen in the SiO_2 lattice to form CO on CO_2. Under conditions of energetic particle bombardment, CF_3 on SiO_2 might be indistinguishable from the same atomic constituents (i.e., C+3F) incident

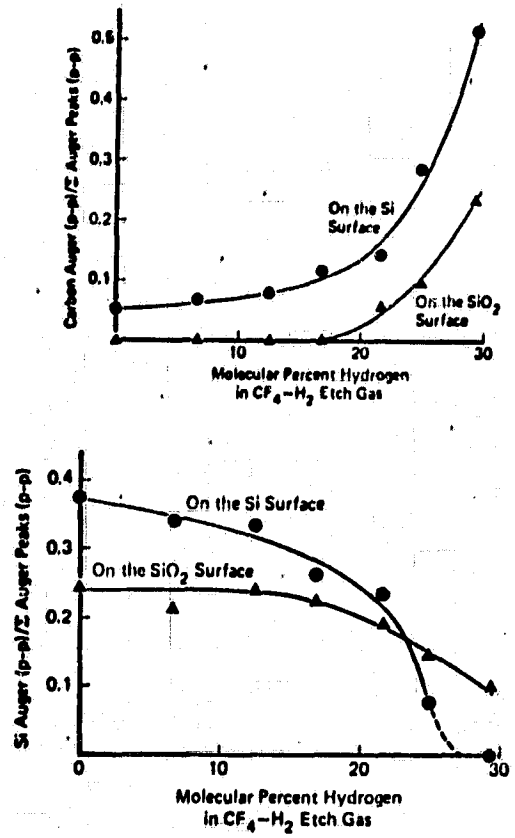


Figure 23. The carbon and silicon Auger peak intensities (normalized with respect to all other observable Auger peaks) on both Si and SiO_2 surfaces as a function of the molecular percentage of H_2 in the CF_4 etch gas. Both the Si and SiO_2 surfaces were rf-biased at a potential of -100 volts during the 5 minute exposure to the CF_4-H_2 discharge. Both surfaces were exposed simultaneously to the discharge and Auger spectra were recorded within minutes of the discharge treatment without air exposure. (Data from Reference 42).

on SiO_2. If this is the case it is somewhat misleading to attribute the etching to the CF_3 radical when in fact the key feature is the disposition of the atomic constituents. On the other hand, if CF_3 radicals etch SiO_2 spontaneously at room temperature, it is perfectly proper to ascribe the etching of SiO_2 to the molecular nature of the CF_3 radical under conditions where the atomic constituents will not react.

b. Active Species Consumption by Etching - The Loading Effect

A major difference between plasma etching and sputter-etching is that in the former, a fraction of the etching gas is consumed in the etching process. The amount of etch gas actually consumer can be quite large as is shown in Fig. 24 [13] in which the Si atom flux and the evolution of SiF_4 are plotted as a function of sample area for several typical etch rates. Consequently the etch gas flow rate is an important parameter in plasma etching. A serious consequence of this consumption of active species is the so-called "loading effect" in which the etch rate decreases with increasing area of etchable material exposed to the plasma [7, 12, 43-45]. An example of the loading effect is shown in Fig. 25 [7] in which the etch rate of aluminum in a CCl_4 glow discharge is plotted versus the area of aluminum surface being etched. The fact that the etch rate is so strongly dependent on the area of etchable material indicates that

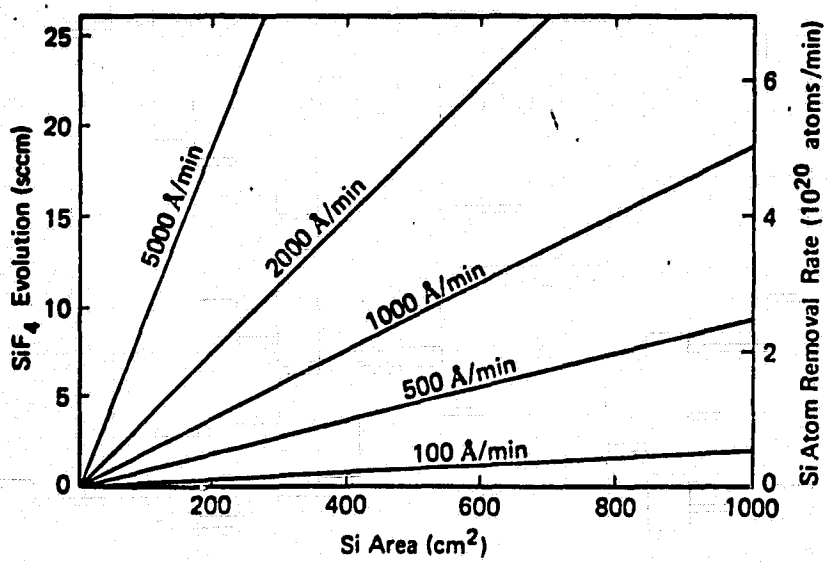


Figure 24. The SiF_4 evolution and the Si atom removal rate as a function of the Si wafer area for several typical etch rates. (See Ref. 13).

the etching process must be the dominant loss process for the etching species - that is the walls of the system must be relatively unreactive to the etching species and relatively few etching species are removed by the vacuum pumping system.

The loading effect is usually a negative factor in the application of plasma etching. Ideally as one approaches the termination of an etch process one would like to have a lower etch rate to facilitate terminating the etching at the correct time, minimizing overetching. However, with a loading effect, as the etching nears completion less etchable material is exposed to the plasma and the etch rate increases. Not only does the etch rate increase but several aspects of the etching process such as selectivity and directionality which depend on the density of the etching species, can also change.

The loading effect problem must be approached by having the etch process consume a relatively small fraction of the etching species. It does not seem feasible to accomplish this by increasing the pumping speed of the pumping system - very large pumps are required to compete with the pumping of active species by a large area of etchable material. A second approach might be to introduce into the plasma a large area of the material being etched (much larger than the area of interest) so that the system is always almost fully "loaded". A third approach, which is being used in certain applications, is to choose an etch gas or etch gas mixture in which the active species are consumed by processes other than etching [46].

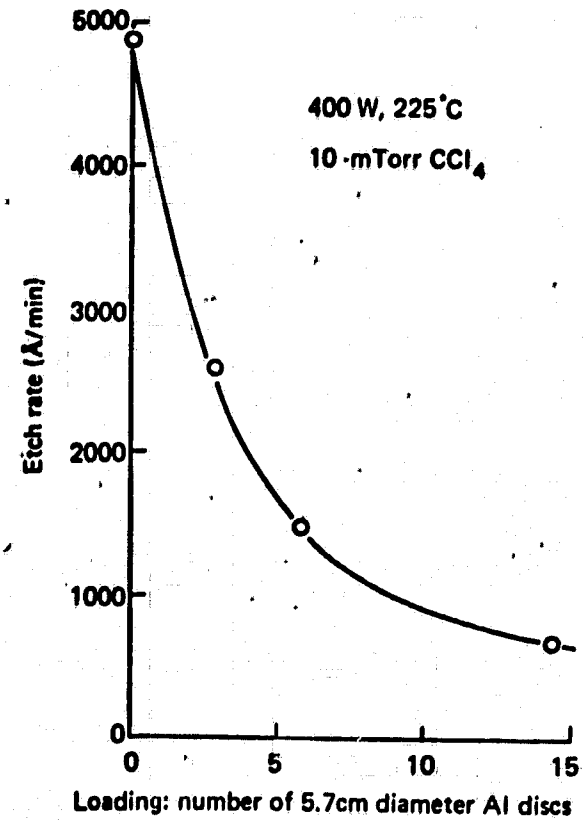


Figure 25. The loading effect (etch rate versus batch size) observed during the etching of Al in CCl_4 in a reactive ion etching configuration (data from Ref. 5).

It is not always the case that a loading effect is a problem. If changes in the etch rate and other characteristics of the etch processes can be tolerated as the etch process nears completion, the loading effect can be used as a basis for an end-point termination.

Whereas silicon in a CF_4 plasma shows a large loading effect, silicon dioxide under similar conditions does not load the system to an appreciable extent even though the amount of SiF_4 evolved in each case may be comparable. The reason for this somewhat puzzling observation is the presence of oxygen in the SiO_2. In the case of SiO_2, the loading effect of the silicon component which tends to

decrease the F atom concentration is approximately compensated for by the presence of oxygen which tends to increase the F atom concentration. The situation can be clarified with the following hypothetical experiment. Place a very small area of silicon in a CF_4 plasma and observe a high etch rate. Add some more silicon to the system and the etch rate will decrease due to the loading effect. Now add some oxygen to the CF_4 etch gas until the etch rate is back up to the initial value. Add more silicon, compensate by adding more oxygen and so on. In this experiment the loadding effect has been eliminated by adding just the correct amount of gaseous oxygen. In the etching of SiO_2, approximately the correct amount of oxygen is evolved in the etching process.

9. Plasma Diagnostics and Process Control

It is not the purpose of this section to attempt a discussion of the general field of plasma diagnostics [47]. This treatment will consider only those experimental procedures which have been used to characterize or monitor plasma etching systems. It would appear at this stage of the development of plasma etching technology that some sort of process monitoring is required. The large parameter space (see Fig. 6) and the sensitivity of the process to uncontrollable factors such as absorbed water vapor make the implementation of this technology without process monitoring a rather risky venture at the present time. The types of measurements that have been made in plasma etching systems consist of two basic types of measurements: (1) Measurements on the surface being etched - either an in-situ etch rate measurement or an end point detection method, and (2) measurements of the concentrations of certain key gas phase species - either etching species or etch product species.

a. In-Situ Etch Rate Measurements

Most measurements of the etch rate in plasma etching technology are not performed in-situ but consist of gravimetric or profilometer measurements performed on the wafers upon removal from the etching system. These approaches are very useful in characterizing an etch process in a developmental stage but cannot be used as a process monitor. The most widely used in-situ etch rate measurement technique is laser interferometry [48] which can be used with optically transparent layers on reflective substrates (e.g., SiO_2 on Si). The reflectivity of a laser beam directed onto

the surface is measured and as the thickness of the transparent film decreases, the amplitude of the reflected beam varies periodically as reflected light from the substrate (e.g., Si) constructively and destructively interferes with light reflected from the outer surface of the transparent film (i.e., SiO_2). In some etching tasks, the area being etched will be too small for good reflectivity measurements and in these cases a larger area test site must be added to the wafer patterning to facilitate this measurement. There still remains the question of whether or not monitoring the etch rate of one wafer is adequate when a large batch of wafers are being processed. In principle the interferometric method could be applied to many wafers but then the questions of how does one stop the etching on specific wafers must be addressed. Hopefully the etching uniformity of future etching systems will be adequate to permit single wafer monitoring.

Laser interferometry can be used in some situations to detect the end point in the etching of an optically opaque layer. In these cases the reflectivity is constant during the etching process, but undergoes a sharp transition when the interface is reached if the reflectivity of the underlying layer differs substantially from the reflectivity of the material being etched. Needless to say, no in-situ etch rate measurement is possible when only the reflectivity of the outer surface of the etched material is being measured.

A second method of monitoring etch rates of any material involves the use of quartz crystal microbalances. This approach is more difficult to implement than laser interferometry particularly

on rf-biased wafers and consequently has been used only in specialized systems [34]. The implementation of this method involves predepositing thin films of the material being etched onto the quartz crystals prior to their installation in the etching system. The coated crystals must then be installed in the discharge and should be operated at the same potential as the wafers being etched. Hopefully, it should be possible to calibrate the wafer etch rate versus the etch rate of the microbalance, the latter being directly indicated as a frequency change during the etching process.

b. Gas Phase Measurements

b.1 Optical emission spectroscopy

Emission spectroscopy has up to this time been the most useful optical diagnostic method. Absorption spectroscopy suffers from the disadvantage of low sensitivity for detecting moecular species at the low concentrations encountered in plasma etching technology. Atomic absorption has good sensitivity, but the species of primary interest (i.e., F atoms) absorb in the experimentally inconvenient vacuum ultraviolet region of the optical spectrum. It is anticipated that the on-going development of stable tunable laser light sources will stimulate the use of absorption spectroscopy and stimulated emission spectroscopies in reactive plasma diagnostics.

Emission spectroscopy already has played an important role in reactive plasma diagnostics [19,32,43,49,50] and is probably the best method for monitoring the relative concentrations of F atoms. It is believed that the F atom concentration is the most useful

single indicator of etching behavior in fluorocarbon plasmas, not only because F atoms are the dominant etching species but also because the F atom concentration is correlated with the concentration of other important species such as CF_3 radicals. That is if the F atom concentration is large, the CF_3 concentration will be small and vice versa. Emission spectroscopy has the additional important advantage that is easily implemented in a plasma etching system. Emission spectroscopy suffers from the disadvantage that the intensity of the emitted light depends not only on the density of the species of interest, but also on the parameters of the glow discharge. That is, $I(F) \propto n(F^*)$ and $n(F^*) \propto k[n_e, f(E)] \cdot n(F_o)$ where $n(F^*)$ is the density of F atoms in the electronically excited state responsible for the light emission I(F), $n(F_o)$ is the density of F atoms in the ground electronic state which is the quantity of interest, and k is a measure of the efficiency with which the glow discharge excites F atoms from the ground state into the optically emitting state. k will be a function of the electron density n_e and the electron energy distribution function f(E) as well as the cross section for the excitation process. The consequence of all this is that the observed signal I(F) is not a reliable measure of the relative F atom density, $n(F_o)$, as plasma parameters are changed.

This difficulty can be overcome to a large extent in the case of F atoms by injecting a small but known amount argon (1-2%) into the CF_4 glow discharge [51] and monitoring the light emission from both electronically excited argon atoms, I(Ar), and from

excited F atoms, I(F). The energy levels responsible for I(Ar) are close in energy to those responsible for I(F) and therefore the value of k relating $n(F^*)$ to $n(F_o)$ should be proportional to the value of k relating $n(Ar^*)$ to $n(Ar_o)$. That is $n(Ar^*) \propto k[n_e \cdot f(E)] \cdot n(Ar_o)$. These expressions can be combined to give

$$\frac{I(F)}{I(Ar)} \propto \frac{n(F_o)}{n(Ar_o)}$$

having cancelled out the k's. I(F) and I(Ar) are measured, $n(Ar_o)$ is known (the partial pressure of argon in the system) and therefore relative values of $n(F_o)$, the F atom density, can be determined as plasma parameters are varied. This approach has the additional advantage of using a ratio of light intensities so that geometrical factors such as collection efficiency, etc., cancel out. It is aticipated that this ratio I(F)/I(Ar) may prove to be a useful characterization or scaling parameter for plasma etching systems.

If, however, one is not concerned with parameter changes, the absolute value of I(F) alone can be very useful. If the etching system is in a loaded condition [43,52] I(F) can be used as an end-point detection scheme - that is I(F) will increase when the area of etchable material decreases.

Optical emission from molecular etch product species can also be used as a process monitoring signal. Species from which optical emission signals have been used in this way include AlCl[49] (in the CCl_4 plasma etching of Al), CO and OH [53] (in the ashing of carbonaceous material), N_2[50] (in the CF_4 etching of Si_3N_4) and SiF [50] (in the CF_4 etching of Si).

b.2 Mass Spectrometry

Mass spectrometric sampling of glow discharges has been a rich source of information for both specific reactions in discharges and overall discharge behavior. Two basic approaches can be used in the mass spectrometric analysis of glow discharge species: (1) Ionic species can be extracted directly from the glow discharge and mass analyzed, or (2) a fraction of the neutral species can be ionized by electron impact after the neutral species have been extracted from the discharge region. Both approaches have advantages and disadvantages and the question as to which approach is most useful is usually answered by a careful consideration of the plasma process being studied.

Both mass spectrometric approaches are much more difficult to implement in a plasma etching system compared to emission spectroscopy. It should be noted that the mass spectrometer is compelled to sample species at a plasma boundary whereas optical emission spectroscopy derives its information from the bulk plasma. This may be considered an advantage for mass spectrometry in that the wafers also are located at a plasma boundary.

The apparatus required to sample the ionic species directly from the glow discharge is more complex than that required for mass spectrometric sampling of the neutral species. The ionic species must be extracted through a small sampling orifice in the wall of the plasma chamber and focussed into the mass spectrometer. Quadrupole mass filters are well suited for this application primarily because these instruments require only low energy ions

(~10eV) and can tolerate a fairly broad energy distribution of the ions. Magnetic sector instruments require that either the plasma itself or the drift tube of the mass spectrometer can be operated substantially away from ground potential in order to obtain the large and often variable ion kinetic energy required by these instruments. In many direct ion sampling experiments, the objective is to sample accurately the ion density in the bulk plasma. Ion-molecule collisions in the sheath region and downstream from the sampling orifice distort this measurement and care must be taken to consider these effects [54]. It should be mentioned that for those situations in which plasma-surface interactions are the primary interest, the collisional processes in the sheath region are no longer a distortion of the measurement but must be included in order to obtain a true picture of the ionic flux incident on surfaces. One method of determining the importance of collisional processes is to place an energy spectrometer between the sampling orifice and the mass spectrometer [55]. Ions coming directly from the bulk plasma will have an energy characteristic of the plasma potential whereas ions formed in the sheath or downstream from the sampling orifice will have a lower energy. Retarding potential techniques can also be used to obtain similar insight into this problem and, although energy distributions measured with retarding potential systems tend to be less precise than those obtained with deflection energy spectrometers, the retarding potential approach is compatible with line-of-sight sampling of the neutral species.

The interpretation of direct ion sampling data can be difficult (see Fig. 8 for an example of an ionic mass spectrum). The relative

ion peak intensities are determined by the cross sections for electron impact ionization of the neutral molecules in the plasma modified by various ion-molecule reactions which can consume the original ion. The ionic species in general will not be proportional to the population of neutral species. Even though the ionic mass spectra contain useful information concerning the etching process, particularly in the etching of materials in which the etch product has a low vapor pressure, it would seem that the complexity of both the instrumentation and the data interpretation will limit the application of this diagnostic method to more research-oriented applications.

This is not true for mass spectrometric sampling of neutral species, an approach which has been used by several workers in the study of plasma etching phenomena [12,13,15,19,33,34,40,56.57]. Neutral species are best sampled using molecular beam methods in which the mass spectrometer ionization chamber is on a line-of-sight with the glow discharge and the effusing neutral beam is modulated by a chopper between the plasma and the ionization chamber. When only the modulated component of the mass spectrometer output is monitored, all neutral species, including reactive radicals can be detected with comparable sensitivity. If modulation techniques are not used, the sensitivity for detecting reactive or condensible species is much less than for noncondensible, nonreactive neutral molecules because of the much larger effective pumping speed for the former in the mass spectrometer chamber. A major problem in the interpretation of neutral mass spectrometry is the fragmentation of high concentration neutral

molecules in the ionization source of the mass spectrometer. For example, F^+ created from the reaction $e+CF_4 \rightarrow CF_3+F^++2e$ usually is much larger than F^+ resulting from $e+F \rightarrow F^++2e$ and most often it is the latter reaction which is of interest. This problem can be approached either by determining the cracking pattern of CF_4 and subtracting out the F^+ signal due to the dissociative ionization of CF_4, or by using low energy electrons which are below the threshold for making F^+ from CF_4 (24eV) but above the threshold for making F^+ from F (17.4eV). Regardless of what approach is taken, it is not a trivial task to detect reactive radicals in plasma etching systems using mass spectrometric detection.

Consequently, the ease of installation of non-line-of-site, nonmodulated, neutral sampling systems has prevailed in most instances. In the etching of silicon and its compounds, the etch product SiF_4 can be detected with good sensitivity and this signal can be used as a process monitor or an end point detection signal [56,57].

c. Miscellaneous Measurements

Although laser interferometry, optical emission spectroscopy and neutral species mass spectrometry are by far the most widely used in-situ diagnostic procedures, several other types of measurements have been used in specific apparatus configurations or to obtain insight concerning plasma etching mechanisms. These specific methods include IR absorption spectroscopy [19] to analyze the effluent gas, molecular chlorine titration to determine the F atom concentration, [19] surface chemiluminescence to monitor

Si etch rates in systems where the etching is performed outside of the plasma zone, optical emission spectroscopy of rotational levels to determine the rotational temperature of the gas [58,59] and in-situ surface analysis of plasma-treated surfaces to obtain mechanistic insight [42]. It is anticipated that none of these special methods will be widely used in the diagnostics of etching plasmas and consequently no detailed discussion will be presented here.

10. Etching of Aluminum and Aluminum Alloys

By comparison with silicon, the etching of aluminum and its alloys is very poorly understood. Aluminum cannot be etched in fluorine-based gases since aluminum fluoride has an extremely low vapor pressure. As a result, chlorine-based gases are almost always used. And this is why the aluminum etching system has seen limited research; chlorine is extremely corrosive and most people either fear for their analytical equipment or are still repairing it from a previous encounter with chlorine! It is assumed that $AlCl_3$ is the volatile reaction product, although this product is not observed by mass spectrometry unless special precautions are taken to ensure that the aluminum trichloride is not condensed before spectrometric sampling.

There are several reports of successful aluminum etching in both high pressure diode [60-63] and reactive ion etching systems [64], but apparently less frequently in barrel reactors. Various gases, including Cl_2, Br_2, HCl, HBr, CCl_4 and BCl_3 [60,64], have been used for aluminum etching with the last two preferred as

CCl_4 - Ar [64], CCl_4 - He [63] or BCl_3 [60,61]. It seems that significant ion bombardment is required to plasma-etch the aluminum, although whether this is really to activate the aluminum - chlorine reaction, or simply to remove the surface aluminum oxide coating, is less clear. It has been proposed that the oxide is reduced by the use of BCl_3 [60], CCl_4 [62], or etched away by sputtering. The use of significant ion bombardment is manifested in the almost exclusive finding of directional etching in aluminum.

It seems that there is far more difficulty in etching with chlorine-based rather than fluorine-based gases. These difficulties are manifested primarily as nonreproducibilities and non-uniformities. Various recipes are offered to overcome these problems. For example, by a CF_4 plasma preclean of the wafer immediately prior to etching [61], or by an initial high power etch [63]. Aluminum and aluminum-silicon seem to be easier to etch than the alloy containing copper, though all these alloys have been etched. The low volatility of copper chlorides makes the effectiveness of wafer heating to 200°C during the etching of copper-containing alloys apparently easy to understand, although the etching has also been achieved without deliberate wafer heating [61].

Metal etching may need post-treatment. One proposal [61] is that Al-metallized wafers should be water rinsed immediately after etching, while the residue on Al-Cu-Si metallized wafers can be removed by rinses in nitric acid, a wetting agent, and deionized water. A second proposal is to follow a CCl_4 - He plasma etching

process with an in situ oxygen plasma clean [65]. Pitting in the sidewalls of RIE-etched aluminum has also been reported [66].

11. Downstream Etchers

Products from an electric discharge can be transported by a rapid flow system from the region where they are created to another region where wafers can be placed. Reactions of free radicals created in this manner have been studied for a number of years in what are often referred to as flowing afterglows, which implies the presence of reactive species giving rise to the luminescence and is common to many systems, particularly those containing atomic nitrogen.

Removal of the discharge zone from the etch region eliminates problems associated with resist degradation and device damage from high-energy particle bombardment. The downstream etchers are similar in this respect to tunnel barrel etchers. Wafers are, however, handled differently. The wafer loading region of a downstream etcher is usually planar as in the ordinary planar plasma etcher. Wafers sit on a heat sink surface and the number of processed wafers depends on the size of the platten. By separating the discharge from the etching region, details of the process such as pressure and geometry can be optimized independently. The operating pressure of the discharge zone can be controlled independently of the pressure in the etching chamber. Generally, the former is high to improve power coupling and efficiency whereas the latter is low to improve uniformity and enhance transport of the reactive component from the discharge.

This approach has several advantages and disadvantages for VLSI processing. The two principal negative features are the limitation (as of this writing) to silicon and nonselective oxide and nitride etching and the totally isotropic character of the etch profiles. Compensating for these, however, are the excellent uniformity and control that can be achieved [67]. In addition, high rate etching can be achieved with essentially no resist degradation, making it attractive for use with thin, process-intolerant resists. The lack of anisotropy probably limits the method to 2-μm or larger geometries, except where exceptionally good uniformity and control can be achieved. In this case, 1-μm critical dimensions might be achieved in 0.5-μm-thick films primarily for polysilicon patterning. It is not clear, however, how this would be in any way preferable to anisotropic etching with the chlorine-containing etchants described in the next section.

12. Ion Milling and Sputter Etching

An energetic ion incident on a solid surface can transfer sufficient energy and momentum to an atom to eject it from the solid [69,70]. If the process is performed in what is traditionally a diode sputtering system, or a reactive ion etcher, it is generally referred to as sputtering [68]. On the other hand, ion milling implies a separation of the ion formation and acceleration system from the region in which the material being processed is placed. The latter system allows direct control over the angle of incidence with which the ions strike the surface This additional degree of freedom is important in obtaining precise control of

contours. The material removal rate and redeposition of sputtered material depend on the angle of incidence of the incoming ions. In the mill configuration this can be varied, while in the normal sputtering arrangement normal incidence is derived from the built-in electric field.

Nonreactive sputter etching, or ion milling, exhibits relatively poor selectivity between different materials and particularly against photoresist removal. This, plus the additional problem of radiation damage, has limited the use of these momentum transfer methods in silicon technology. Milling does have significant application in the manufacture of such devices as bubble memories, surface wave devices, integrated optics, and nonsilicon-active materials, where fine geometries are encountered as microwave FETs and the materials are not amenable to plasma etching.

Also, films such as aluminum alloys containing 4% copper are difficult to etch by planar plasma or RIE because of the high vapor pressure of the copper constituents at room temperature. Currently the substrate temperature must be raised to 200°C which promotes organic resist degradation. Ion milling and reactive ion milling show promise for etching these films.

13. Dry Etching System Comparison and Key Operational Parameters

A comparison of the typical dry etching systems is shown in Figure 26 which illustrates the various reactor geometries [71]. Also, Table II gives typical applications for the more common system configurations.

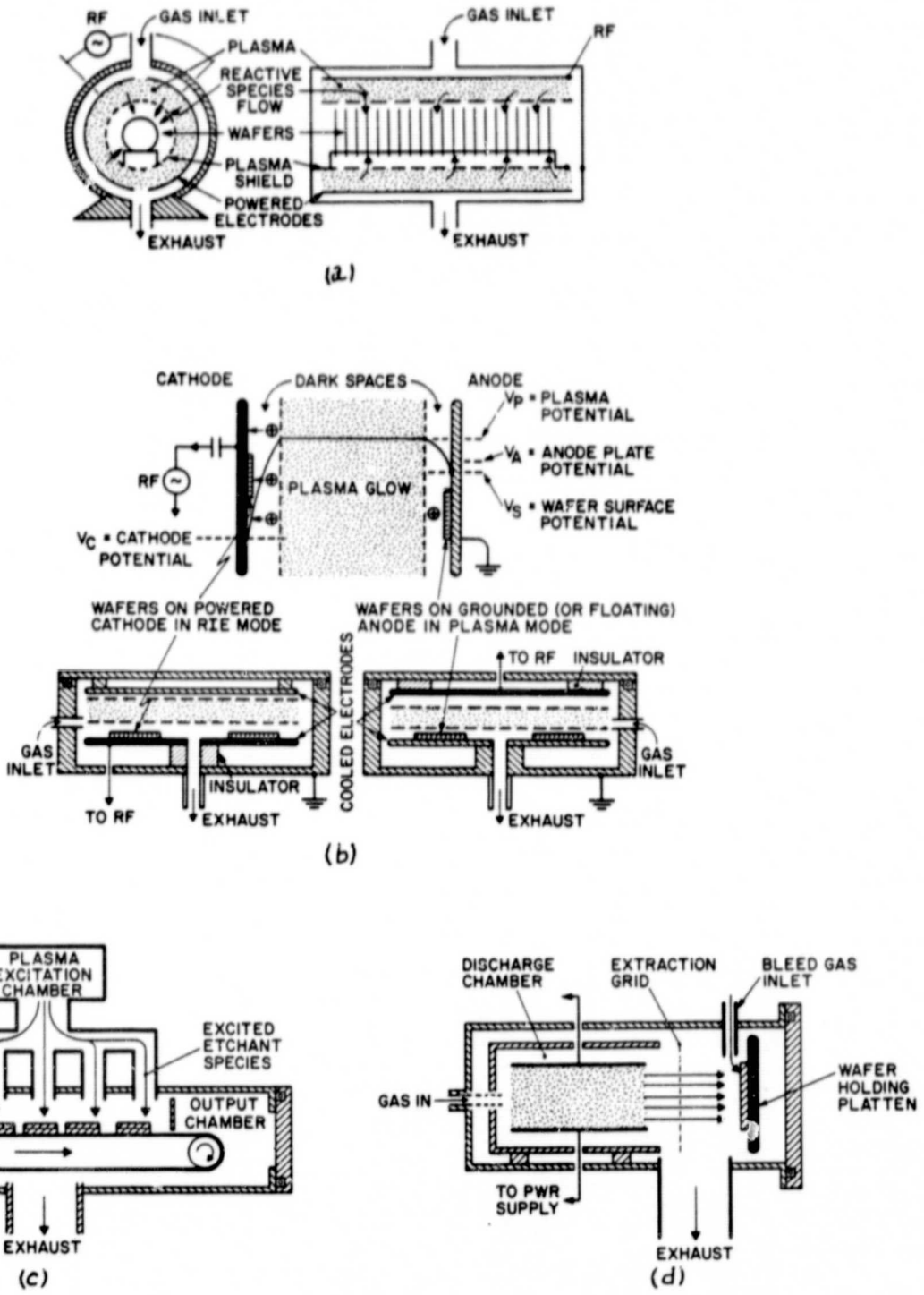


Figure 26. A Comparison of Dry Etching System Configurations, (a) Barrel Etcher Configuration, (b) Planar Plasma/Reactive ion Etch Configuration, (c) External Generation, Continuous Flow Reactor Configuration, and (d) ion Milling Configuration.

TABLE II

APPLICATIONS OF SYSTEM CONFIGURATIONS

CONFIGURATION	APPLICATION	COMMENTS
Barrel	Photoresist stripping, selective etching of polysilicon and silicon nitride with geometries of 5 μm or more.	Isotropic etch profile
Planar	Selective etching of polysilicon, silicon nitride, refractory silicides, SiO_2 and Al, with geometries from 5 μm to submicron.	Anisotropic or isotropic depending on operating conditions and gases used.
RIE	Selective etching of silicon dioxide where high selectivity to silicon is needed (CF_1 and H_2 gases).	Anisotropic etching/high selectivity/low polymer formation.
ion milling	Special/unusual submicron etching of inert films.	R&D/limited use in production.

A qualitative comparison of various dry etch processes (including comparison of wet chemistry) is presented in Table III.

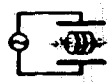
The key operational parameters of a dry etch process are selectivity, anisotropy, uniformity, and etch rate. Selectivity, which is the ability to etch a layer and stop on the underlying material, is a strong function of the chemical species produced in the discharge as well as the physical geometry of the apparatus.

As mentioned earlier, there is general belief that anisotropy results from some form of directed energy normally incident on the surface [72]. If the incident particles are charged, they can be affected by variations in electric field direction near the surface of the workpiece [73]. Local field concentration can increase the ion or electron flux.

Etch rate is important, especially in large volume production. Rates are limited by the reactant supply [74,75], the available usable power for dissociation into active species, and the physical limitation due to resist or mask erosion. Also, for reasons not yet understood, some processes work better at slow rates while others do better when made faster. For example, it is often observed that oxide-to-silicon selectivity improves at low etch rates. The relative rates for the different processes are approximate. Actual values depend on many factors such as loading time, pump out time, and wafer load size, as well as actual film removal rate. Systems can be found for which these differences are less significant.

TABLE III

OPERATING CHARACTERISTICS OF DRY PROCESSING METHODS

PROCESS		WET CHEMISTRY	PHYSICAL SPUTTERING & ION MILLING	PLASMA ETCHING			REACTIVE ION ETCHING
				BARREL	BARREL	DIODE	
WAFER LOCATION		IMMERSION	CATHODE	IMMERSION	TUNNEL	ANODE	CATHODE
SYSTEM SCHEMATIC							
ACTIVE SPECIES PRESENT	High-Energy Ions	✓					✓
	Low-Energy Ions			✓		✓	
	Long-Lived Radicals			✓	✓	✓	✓
	Short-Lived Radicals			✓		✓	✓
	Atoms & Molecules			✓	✓	✓	✓
CHEMICAL SELECTIVITY		EXCELLENT	POOR	GOOD	FAIR	GOOD	GOOD
ANISOTROPY OR LACK OR UNDERCUTTING (DETERMINES RESOLUTION)		POOR	EXCELLENT	VARIABLE	POOR	GOOD TO EXCELLENT	EXCELLENT TO GOOD
ETCH RATE		FAST	SLOW	FAST	FAST	FAST	SLOW
WAFER TEMP. CONTROL		EXCELLENT	GOOD	POOR	FAIR	GOOD	GOOD
MOS DELECTRIC D'M'GE		NEGLIGIBLE	SIGNIFICANT[a]	SLIGHT[b]	NEGLIGIBLE	SLIGHT[b]	SIGNIFICANT[a]
REDEPOSITION		NEGLIGIBLE	SIGNIFICANT[c]	SLIGHT[d]	NEGLIGIBLE	SLIGHT[d]	SIGNIFICANT[c]
ETCH RATE UNIFORMITY		GOOD	GOOD	VARIABLE	GOOD	VARIABLE	GOOD

a. Ion bombardment.
b. UV, electron bombardment, backscattering contaminants.
c. Backscattering of sputtered nonvolatiles.
d. Surface decomposition of radicals, backscattering of contaminants.

Dielectric damage, resulting in enhanced electron trapping in MOS devices, can be produced by penetrating and nonpenetrating radiation [76]. The only methods totally immune to these effects are the downstream etchers and, to a slightly lesser extent, the tunnel, or shielded, reactors.

Redeposition can occur from two different sources. First, material being etched can backscatter by gas collisions onto the surface. This can occur at pressures greater than about 0.1 Torr. Second, material from any other part of the chamber can be sputtered onto or react with the chemically active plasma and transported to the wafers. Some material is particularly susceptible to this type of transport. For example, gold can contaminate a chamber making it useless for etching-sensitive MOS devices [77] without drastic clean up procedures.

All the dry etch methods can be configured to produce uniform etching across a wafer for some processes. Nonuniformity can occur as batch-to-batch, wafer-to-wafer, or intrawafer effects. Batch-to-batch variations may be due to differences in material or changes that occur in the reactor. Important process parameters include gas flow and concentration, pressure, discharge power, and temperature. In addition, some processes modify the surface of the reactor, coating them with a polymericlike material which can make them reactive surfaces that absorb atmospheric gases and interfere with the etch process. Precise control of these variations is difficult and requires sophisticated monitoring apparatus such as mass spectrometers.

Nonuniformity due to material variations between batches can be accommodated by end point detection. Wafer-to-wafer nonuniformity may occur in batch reactors because of variations in process environment such as positional variations in the etcher. In some processes this can be minimized by careful adjustment of process parameters or selection of appropriate operating points. Generally, low pressures tend to reduce positional variations due to gas flow effects. For processes that are essentially chemical, concentration gradients due to loading effects [78] are probably the most significant cause of differences between wafers. They also account for some of the intrawafer variations seen in immersion barrel reactors. For ion-induced processes, variations in current density with position due to edge effects of electrodes and the proximity of alternate conduction paths can produce wafer-to-wafer as well as intrawafer variations. Some batch reactors attempt to minimize positional variations by moving wafers so that they sample different positions in the reactor. It is not entirely clear, however, whether in some processes the physical cause of nonuniformity stays in place with the reactor or moves with the wafer. An example of the latter is the case of radial etch gradients that occur across a wafer, independent of location. This often causes wafers to etch faster at the periphery and clear last at the center and is due to the difference in material between the wafer and support structure. For planar plasma etchers the radial nonuniformity may occasionally reverse its direction with the center of wafers etching faster than the edges. This phenomenon is interpreted as evidence that the supporting table is a sink for reactive components of the plasma.

These variations are significant for the manufacture of VLSI devices if the feature size and/or etching of underlying material is adversely affected. In order to protect the underlying film, high selectivities are necessary if the system exhibits poor uniformity. At first it would seem that high selectivity and anisotropic etching are all that are required to give good patterning, independent of uniformity, and for some processes this is true. There are, however, a number of situations when high selectivities are not possible, for example, in etching an oxide film that terminates on another oxide layer of different composition.

An intrawafer nonuniformity effect that may be of significance as geometries shrink is a microscopic size effect. It is manifested as different-sized geometries etching at different rates. Smaller areas may etch faster than large ones or vice versa. Most likely it is due to a miniloading effect with the resist mask playing an active role in the etch process. If the mask is nonreactive to etching species, the concentration of etchant is greatest near the mask edge and near small geometries, which therefore etch faster. If the mask is a sink, the opposite situation prevails. If this problem is encountered, it may be necessary to ensure that critical lithographic steps do not contain grossly diverse feature sizes.

The problem of intrawafer nonuniformity will most likely increase with increased wafer size. It may make some of the newer, single-wafer processing systems more attractive. In this type of reactor, each wafer is processed individually, obviating effects associated with placement in a batch reactor. Additionally, if intrawafer nonuniformities exist, they can be adjusted for by

adjusting gas flows, discharge plates, or other geometrical arrangements.

Typical etching gases used for silicon and silicon-dioxide are presented in Tables IV and V.

TABLE IV

SILICON ETCH GASES

GAS	SYSTEM	FEATURES
CF_4	All	Isotropic but depends on condition
$CF_4 + O_2$ (1-10%)	All	Enhanced silicon rate
$CF_4 + O_2$ (20-50%)	Downstream	Isotropic, highly selective versus SiO_2
CCl_4, Cl_2	Planar, RIE	Anisotropic
$SiF_4 + O_2$	Barrel	Less isotropic than CF_4
$CF_3Br + C_2F_6$	Planar	Anisotropic

TABLE V

SiO_2 ETCH GASES

GAS	SYSTEM	FEATURES
CF_4	Planar, RIE	Selectivity depends on conditions
$CF_4 + O_2$ (1-10%)	Planar, tube	Fast, but silicon must faster; variable anisotropy
$CF_4 + O_2$ (20-50%)	Downstream	Isotropic, temperature-dependent rate much slower than silicon
$CF_4 + H_2$	Planar	Selective against silicon
C_2F_6	RIE	
C_3F_8		
CHF_3		

14. Present Trends

Considerable interest is being shown in anisotropic etching, careful control, and more monitoring of the entire etch process. Ion-dependent processes such as reactive ion etching are receiving much more attention and the first generation of commercial equipment to perform RIE is becoming available. The main goal is geometry control, but if this can be achieved by other techniques, they will be used if the overall cost is lower with substantially the same yield. Larger wafers are making batch reactors that etch several wafers at a time less attractive in comparison with one-at-a-time wafer etchers, several of which are being manufactured and sold. If process speed can be increased to make their throughput (per unit equipment cost) equivalent to batch reactors, they will see extensive application in manufacture for several processes.

Designers of new resist systems and lithographic tools are now asking if their processes are compatible with dry etching. Dry etching is changing from a replacement for wet etching to a dominant, controlling factor in process flow. It is likely that the dry etching methods and the results they produce will reach one step further back in device design and begin to impact the basic device architecture. Those organizations that are able to integrate this information into their device design structure will have a distinct competitive advantage.

B. Dry Deposition Processes

1. Introduction

As indicated, applications of plasma chemistry to semiconductor processing is just beginning to realize its potential. For deposition processes, plasma chemistry is also playing an important role in replacing traditional methods of depositing dielectric and semiconductor films by high temperature processes.

The following terms are used to describe this thin film process: plasma deposition, plasma polymerization, plasma enhanced CVD (PECVD), and glow discharge deposition on polymerization. The uniqueness of the plasma to generate chemically reactive species at low temperatures is due to the non-equilibrium nature of the plasma state. Non-equilibrium means a gas plasma typically sustained at 0.1 to several Torr, which exhibits temperatures of the free electrons of tens of thousands ^{o}K, while the temperature of the translational and rotational modes of free atoms, radicals, or molecules will be only hundred ^{o}K. Thus many of the limitations of high temperature CVD processes at approximately 1000°K can be greatly relaxed, due to plasma-generated energetic electrons, to lower temperatures of ambient to approximately 500°K.

By far the greatest amount of published literature regarding thin film formation in a plasma is related to organic or organometallic polymeric thin films. This is because of the usual greater experimental ease of production [79] and the easy accessibility of the readily polymerized monomer. Some initial work had been done in the early 1960's with inorganic films produced

by plasma and with both organic and inorganic film studies. During this period, film properties became much better characterized and some of their potential industrial applications were identified. The objective of much current research at present is the development of processes and equipment to attain controlled film properties over a larger total substrate area for production applications.

In the design of experiments or equipment, the dominant plasma parameters affecting deposition rate, uniformity, and film qualities must be identified. What is generally most critical in terms of these requirements is summarized in Figure [27]. The three principal considerations are the gas kinetic processes, the electrical configuration used to produce the plasma, and the conditions or disposition of the substrate interfacing with the plasma. Obviously, as with most vacuum processes, the gas flow rate, pressure, and gas-flow pattern are critical. These requirements are met by the design of the specific reactor employed.

The electrical system to generate the plasma has several well-understood and poorly-understood aspects. Well understood are the various geometries of the electrodes, either internal or external relative to the reaction zone, to establish a homogeneous plasma. Less well understood is the effect of frequency on the plasma process. The electrical and plasma interaction with the substrate is in some aspects difficult to probe. Current collection at the surface (amps/cm^2) is either measurable or can be calculated if one knows the electron and ion density.

When a low temperature plasma interacts with a solid surface, a number of energy and mass transfer processes take place

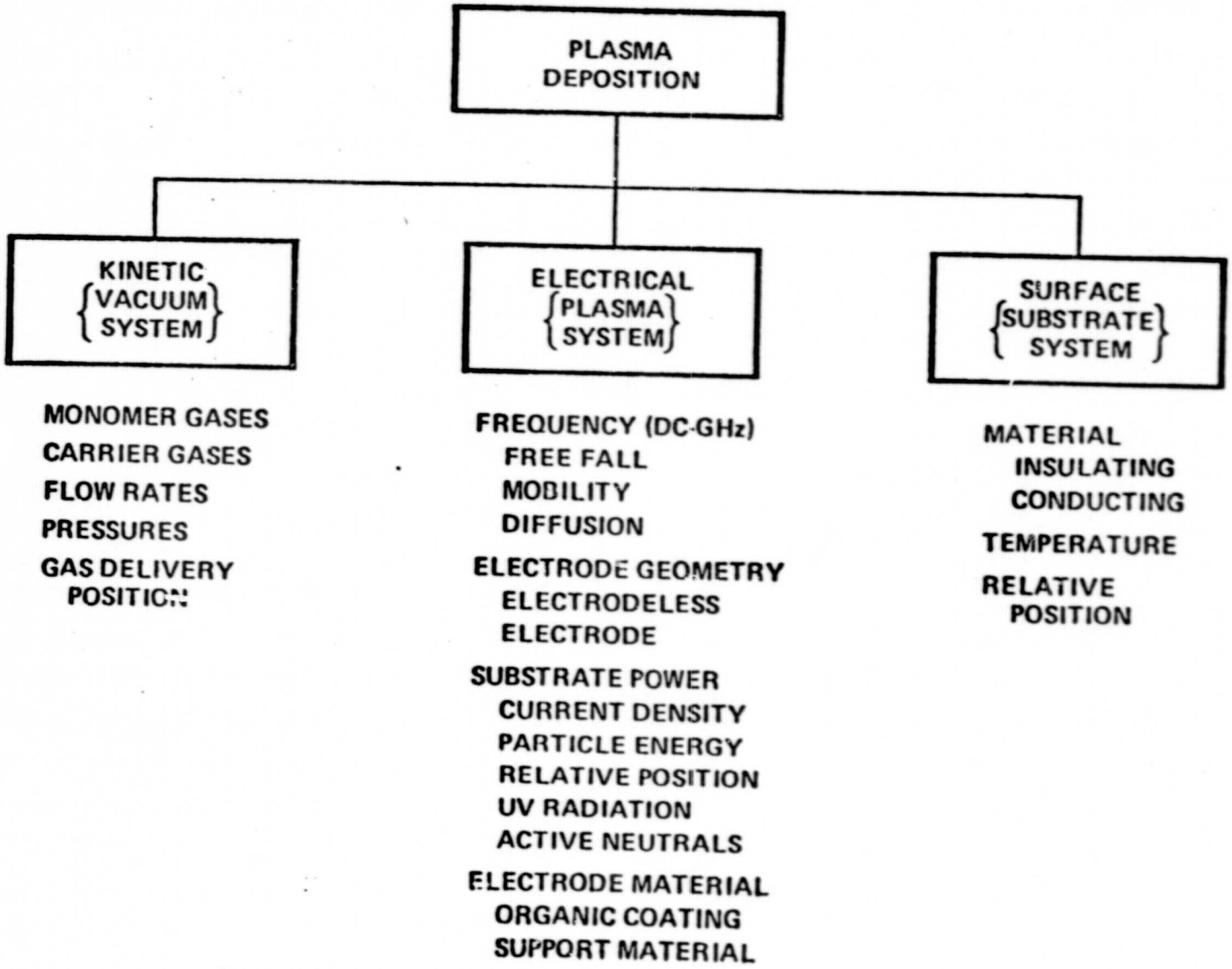


Figure 27. Dominant parameters affecting plasma deposition: vacuum, electrical, and sample systems.

concurrently which produce the final surface and film properties. The two main types of interactive mechanisms are radiation and particle fluxes to the surface. The radiative mechanism consists for the most part of IR, visible and ultraviolet energy interaction. The ultraviolet interaction is the most energetic and can be responsible for considerable contribution to gas phase reactions. Particle fluxes consist of electron, molecule ion, atom, atomic ion, free radical, and undissociated or non-ionic species depending on the initial gas composition. Ground as well as excited state interactions are also possible in the particle reactions or bombardment of surfaces.

Studies [79] on plasma film formation have generally treated the various particle and radiation interaction processes cooperatively. Very little has been done to date to separate the various roles that each type of energy or mass transfer interaction may have on the surface. To separate the contribution of each particle and energy source to the total surface modification is indeed difficult due to the numerous species that exist in plasmas.

The conditions of the substrate surface can greatly affect the film formation rate and uniformity. As in other thin film processes, film adhesion is governed to a large extent by surface cleanliness. This can be insured in plasma processes by first pre-cleaning the surface with an oxygen discharge if it is compatible with the substrate. Temperature of the substrate and its position relative to the reaction zone can significantly affect the deposition rate. Rates can increase or decrease as substrate temperature rises. The more closely localized the plasma reaction zone

relative to the substrate surface the greater will be the deposition rate. However, the film qualities are also affected by this proximity. After initial experiments, the optimization of deposition rate, refractive index, stoichiometry, etc. can be achieved in most cases.

2. Requirements and Techniques for Plasma Thin Film Production

a. Reactor Design

Every flow discharge system that is capable of thin film production is comprised of the following basic components: 1) the reactor or reaction chamber, 2) a vacuum pumping station, 3) a gas flow and control section, and 4) electronics -- power source, matching network, and pressure gauge plus other instrumentation.

Broadly speaking, the two general types of reactor design in most general use are those built around the "planar" or parallel-plate internal electrode configuration, and the tube or barrel-type reactor which most commonly is electrodeless (external electrodes). The planar reactor is more readily modeled and comparable to other planar reactors in terms of performance even though some minor design variations may exist (electrode spacing, gas flow pattern, etc.).

Tube type reactors usually consist of a silica tube from a few cm to perhaps 45 cm in diameter arranged either horizontally or vertically in the overall system. The majority of studies in plasma deposition have utilized medium to high source frequency (KHz to MHz) power supplies. This enables the facile coupling of power into the reactor zone by electrodeless techniques.

There is no equipment available at present which offers the amount of automation, throughput and film quality required by production users. Many production limitations of plasma enhanced deposition systems come about because wafers are processed in a face-up, horizontal position. This makes them susceptible to particulate precipitation and places limits on the batch size. Until recently, available plasma enhanced deposition production systems were variations on the original planar (horizontal), radial flow reactor design, and design changes were attempts to reduce particulates and increase wafer capacities.

Now equipment based on a new design concept is available from two vendors. This equipment processes wafers in a multi-level, vertical, longitudinal flow reactor. Because this system is similar to the widely accepted resistant-heated ("hot wall") LPCVD system, with its inherent advantages from processing wafers vertically, it appears likely that this new design will succeed in dramatically improving plasma deposition processing productivity and quality.

The basic planar, radial flow reactor design is shown in Figure 28. The horizontal parallel plates are electrodes separated by a given distance. This provides a uniform power density at the deposition surface and ensures that all wafer surfaces are exposed to the same reactive species--helpful features in achieving uniformity. Through a matching network the upper high voltage electrode is connected to an RF power supply. The lower electrode which supports the wafers is grounded, and this electrode also heats the wafers through externally-mounted resistant heaters. The lower electrode rotates to permit randomization of wafer position, another factor in wafer-to-wafer deposition uniformity.

From the center of the reactor reactant gases enter and flow radially between the two electrodes. Reaction by-products and unreacted gases exhaust into a circumferential plenum. In order to provide pressure control within the reactor independent of total gas flow, a dual stage pumping system is used. Reactor pressure is monitored in the exhaust plenum and used to control the first-stage variable-speed booster pump. Then exhaust from the booster pump feeds the second stage, which is a standard mechanical vacuum pump. With this dual pumping arrangement, wide ranges of gas flows and pressures may be achieved.

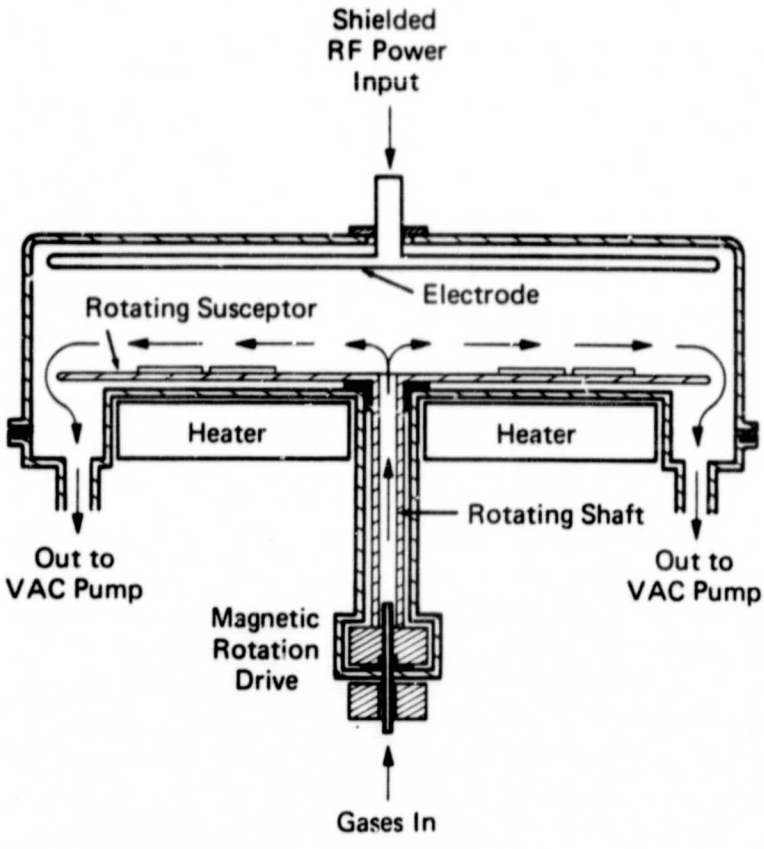


Figure 28. Cross-sectional view of the planar reactor.

b. Silicon Nitride Deposition

To date the principal application of planar reactors has been for the deposition of silicon nitride. PD of silicon nitride has become accepted as the preferred final passivation layer for semiconductor devices, because it provides ionic barrier protection, hermeticity and freedom from moisture-induced metallization corrosion resulting from passivating techniques that use phosphorus-doped silicon dioxide.

Silicon nitride is produced by the reaction of nitrogen, ammonia and silane. Some systems use a silane and nitrogen only reaction. While the practical differences between these two reactions have not been clearly demonstrated, there seems to be a difference in the molecular make-up of the respective nitrides. It is apparently a question of silicon-to-nitrogen concentration in reaction, and the inclusion of hydrogen and/or oxygen in the makeup of silicon nitride.

Odd stoichiometry is one of the traits that makes plasma deposited silicon nitride different from nitride deposited by other means. Rather than the desired Si_3N_4, the films obtained are often reported as $Si_xN_yH_z$ or $Si_xN_yH_zO$ because the exact chemistry is not known. Study is needed to determine exactly how such things as hydrogen incorporation into the film, or incorporation of other species left over from the reaction, are going to affect the long-range processing of a film and the long-range properties of the IC that the film is put on.

The rate of film deposition in Figure 29 is primarily a function of input power level. At higher SiH_4 flow rates, this relationship is linear within the range of the reported experimental conditions. At low SiH_4 flows, particularly when combined with reduced total gas flow, the rate of film deposition tends toward an asymptotic value at higher power input levels. Deposition (wafer) temperature is 240°C. It is to be noticed that, depending on gas flow and composition, deposition rate can either be strongly dependent or independent of power level above a certain point. Reactor characterization for deposition of materials other than silicon nitride would have to take this into consideration.

Under flow conditions that provide uniform deposition, the rate of film deposition can be controlled by variation in the input power without materially affecting the radial uniformity of deposition. The condition of 600 sccm N_2, 300 sccm NH_3 and 150 sccm SiH_4 at 500 watts provides a ± 1.6% uniformity in the deposition zone. A ± 40% change in power level causes only a modest increase

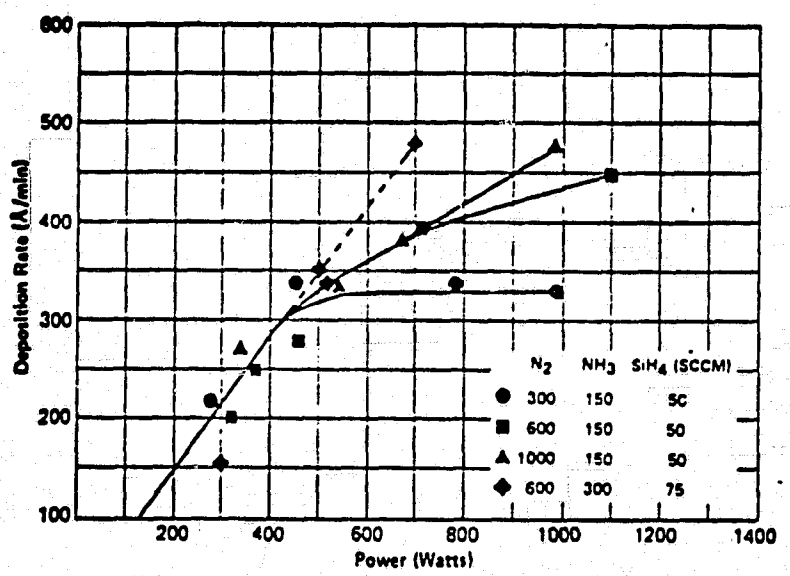


Figure 29. Deposition rate dependence on RF power delivered to the plasma.

TABLE VI

CHEMICAL AND PHYSICAL PROPERTIES OF SILICON NITRIDE FILMS

Properties of Silicon Nitride Films From $SiH_4 + NH_3 + N_2$

PROPERTY		HIGH TEMP NITRIDE 900°C	PLASMA DEP. NITRIDE 300°C
Composition		Si_3N_4	SiN_x
Si/N Ratio		0.75	0.8-1.0
Solution Etch Rate			
Buffered HF	20-25°C	10-15 Å/min	200-300 A/min
49% HF	23°C	80 Å/min	1500-3000 Å/min
85% H_3PO_4	155°C	15 Å/min	100-200 A/min
85% H_3PO_4	180°C	120 Å/min	600-1000 Å/min
Plasma Etch Rate			
92% CF_4-8% O_2, 700W		600 Å/min	1000 Å/min
Na^+ Penetration		< 100 Å	< 100 Å
IR Absorption			
Si-N Max.		~ 830 cm^{-1}	~ 830 cm^{-1}
Si-H Minor		-	2200 cm^{-1}
Density		2.8-3.1 g/cm^3	2.5-2.8 g/cm^3
Refractive Index		2.0-2.1	2.0-2.1
Dielectric Constant		6-7	6-9
Dielectric Strength		1×10^7 V/cm	6×10^6 V/cm
Bulk Resistivity		10^{15}-$10^{17}\Omega$ -cm	$10^{15}\Omega$ -cm
Surface Resistivity		$>10^{13}\Omega$/sq.	$1 \times 10^{13}\Omega$/sq.
Intrinsic Stress		$1.2\text{-}1.8 \times 10^{10}$ dyn/cm^2 Tensile	$1\text{-}8 \times 10^9$ dyn/cm^2 Compressive
Thermal Expansion		4×10^{-6}/°C	
Color, Transmitted		None	Yellow
Step Coverage		Good	Conformal
H_2O Permeability		Zero	Low-None

in the radial uniformity profile. As pressure in the reactor increases, the deposition rate decreases steadily over the range studied of 0.1 - 0.8 Torr. This general behavior is common in plasma deposition, and results from gas phase recombination at higher pressures reducing the availability of reactive, film-producing species.

The typical chemical and physical properties of plasma deposited nitride are listed in Table VI. It is to be noted that the as-deposited films are in compressive stress with a value of about 2×10^9 Dynes/cm^2. This compressive stress, in all probability, accounts for the ability to deposit films exceeding 30,000 Å in thickness which do not exhibit cracking on thermal cycling through 450°C. As might be expected for a low pressure CVD process, step coverage is conformal with excellent coverage even over 10,000 Å steps.

c. Silicon Oxide Deposition

In plasma oxide deposition, N_2O produces, along with other species, atomic oxygen which reacts readily with silane to form SiO_2. This reaction takes place not only on the electrode surfaces and reactor walls but also in the gas phase, which may lead to poor step coverage, high particulate density and other localized structural defects. For optimum film properties, gas phase reactions must be suppressed and surface reactions enhanced by balancing gas composition and rf power density. The process conditions needed to achieve this are a relatively low rf power (150-250 watts) and an N_2O/SiH_4 ratio of 40-60. The resulting films contain some nitrogen but have excellent mechanical and good electrical properties [80].

Typical process conditions for silicon dioxide and silicon nitride in the AMP 3300 system are listed in Table VII.

TABLE VII

Typical Process Conditions for Plasma Oxide and Plasma Nitride in the AMT Plasma Deposition System

	Silicon Dioxide	Silicon Nitride
Gases	$SiH_4 + N_2O$	$SiH_4 + NH_3 + N_2$
% SiH_4	2%	9%
% N_2O, NH_3 resp.	98%	45%
RF Power Density	0.05 W/cm^2	0.17 W/cm^2
RF Frequency	57 kHz	57 kHz
Operating Pressure	53 Pa	33 Pa
Substrate Temperature	300°C	300°C
Deposition Rate	60 nm/min	38 nm/min
Film Uniformity	± 5%	± 4%
Film Composition	$SiO_{1.9}N_{0.15}$	$Si_{3.2}N_4(H)$
Refractive Index	1.54	2.02
Film Density	2.38 g/cm^3	2.75 g/cm^3
Etch Rate (B.O.E.)	130 nm/min	20 nm/min
Etch Rate (CF_4+O_2 plasma)	10 nm/min	150 nm/min

In Table VIII the film properties of CVD SiO_2, plasma oxide and plasma nitride are compared.

TABLE VIII

SOME PROPERTIES OF CVD SiO_2 , PLASMA OXIDE AND PLASMA NITRIDE

	CVD SiO_2	Plasma Oxide	Plasma Nitride
Pinhole Density	1-10 cm^{-2}	$\leq$ 1 cm^{-2}	$\leq$ 0.5 cm^{-2}
Particulate Density	10-100 cm^{-2}	$\leq$ 0.2 cm^{-2}	$\leq$ 0.2 cm^{-2}
Step Coverage	poor	conformal	conformal
Ashesion to Al	good	good	good
Adhesion to Au	bad	good	good
Crack Resistance	poor	good	excellent
Intrinsic Film Stress	tensile $6-8 \times 10^8$ dynes/cm^2	compressive 2×10^9 dynes/cm^2	compressive 4×10^9 dynes/cm^2
Breakdown Voltage	8×10^6 V/cm	8×10^6 V/cm	2×10^6 V/cm
Film Resistivity	> 10^{17} ohm-cm	> 10^{17} ohm-cm	2×10^{16} ohm-cm
Dielectric Constant (1MHz)	3.8	4.6	7.0

d. Silicon Oxynitrides

By proper admixture of NO or N_2O to the silane-ammonia mixture used in silicon nitride production, silicon oxynitride SiO_xN_y can be formed. Very little has been published on this material [79]. By variation of the gas flow ratio one can arrive at compositions of SiO_xN_y which are intermediate between silicon oxide and nitride [81]. One can "tailor" the film composition with respect to stoichiometry, density, refractive index, and etch rate. The oxygen content can be correlated with the index of refraction which varies from 1.5 - 2.0 for films deposited at 400°C as the oxygen contained in the material diminishes. The true advantage of SiO_xN_y compared to plasma nitride is yet to be elucidated.

e. Metal Oxides

e.1. Al_2O_3

Aluminum oxide films have been prepared in a plasma by both vapor phase deposition and by anodization in an oxygen plasma. The interest in aluminum oxide relates to the resistance to ionizing radiation resistance and the large positive value in flat band voltage that this film exhibits. Zaininger and Waxman [82] prepared Al_2O_3 by first depositing aluminum on silicon substrates and subsequently plasma anodizing them in a bell jar type system at 0.3 Torr. The aluminum substrates were located in the positive column of the d.c. plasma. Oxide films of 500-1000 Å were grown at 22 Å/V with the growth ultimately becoming self-limiting. MOS capacitors and transistors were subsequently

fabricated. The radiation-resistant properties of these plasma-produced films were quite remarkable. MOS devices exposed to up to 1 x 10^{13} e/cm^2 electron fluxes under positive or negative bias displayed no oxide charge buildup and no interface state generation. MOS transistors exposed to 1-MeV electrons displayed essentially little shift or deterioration of transistor characteristics.

In a more conventional experiment, Al_2O_3 was prepared in a high frequency 400 KHz vertical tube plasma reactor [83]. Amorphous films of Al_2O_3 were formed by vaporizing $AlCl_3$ into an oxygen plasma. Pressure of the discharge and the $AlCl_3$ vaporization rate greatly affected the rate of film formation, which varied from 70 to 500 Å/min. Rate was linearly dependent on RF power over the range studied. Adherent films up to several μ thick were prepared at the optimum substrate temperature of 480°C. Al-Al_2O_3-Si structures were prepared and characterized as having large positive flatband voltage shifts of up to 40 V, under negative bias at elevated temperature. This implies these films will show high resistance to Na^+ ion diffusion unlike SiO_2. Other film properties such as resistivity, and dielectric constant and strength were acceptable or compared well with thermal oxide prepared from aluminum triethoxide decomposition.

e.2. Oxides of Ge,B,Ti, and Sn

Clear amorphous, glassy films of several metals were prepared [83] by microwave discharge decomposition of the corresponding metal alkyls or alkoxides. Films were typically produced at 0.24 Torr on NaCl substrates (for infrared spectroscopic studies) at 200°C. Growth rates were low, about 20 Å/min.

However, not enough study was done to determine whether these rates could be made higher.

f. Miscellaneous Films

f.1 BN

Boron nitride thin films have been prepared [85-86] by reacting B_2H_6 and NH_3 [86]. High quality films were achieved. They were smooth and transparent, and were found to have better crystalline quality than the material obtained by NH_3 + B_2H_6 by high temperature CVD. The interest in these BN films was based upon their potential for certain microwave devices. However, the hoped-for large carrier drift velocity was not found in these films. Deposition temperatures were fairly high 700-1000°C. Growth rates were quite high 3000 to 7000 Å/min at pressures 0.3 to 1.0 Torr. The best films were produced at a NH_3/B_2H_6 ratio of 8:1.

f.2 P_3N_5

By directly vaporizing elemental phosphorus in a nitrogen plasma, transparent, glass-like films of phorphorus nitride from 0.5 to 10 μ in thickness were produced on a variety of metal and glass substrates [87]. Conditions of film formation were: reactor, horizontal tube; pressure, ~ 1.0 Torr; power, to 500 W; frequency, 25 MHz; deposition temperature, ~ 265°C. Electrical properties were evaluated and permittivity at room temperature was found to be 4.4, independent of frequency. Dielectric strength between 0.3 and 0.5 x 10^7 V/cm was found for samples which had been cycled through temperature extremes of - 196 to 230°C.

3. Applications of Plasma Deposited Silicon Dioxide and Silicon Nitride

a. Device Passivation

Plasma nitride has become the preferred passivation layer for both professional and consumer devices. It provides hermeticity, ionic barrier protection, and prevents aluminum shift in plastic packages. To date the only reported drawback has been a parameter shift in short channel MOS devices which has been related to the outdiffusion of the weakly bonded hydrogen in the nitride films [88,89]. This phenomenon can be minimized by optimizing the deposition conditions, or can be avoided by using plasma oxide in place of nitride.

For optimum device protection a compressive stress of $2 - 5 \times 10^9$ dynes/cm^2 in the passivation layer is needed, yielding excellent mechanical strength and a low pinhole density. Higher stresses, however, will cause a deterioration in device reliability. The maximum allowable initial stress is determined by the stress concentration at steps and windows.

b. Dual Layer Isolation

Plasma oxide and nitride are both outstanding for dual layer isolation. They have a low particulate density, adhere well to Si, SiO_2, Al and Au and, in contrast to CVD SiO_2, provide acceptable step coverage of the top metallization.

For most devices plasma nitride offers advantages over plasma oxide due to its impermeability to moisture and ions; in addition the deposition process is less critical (no gas phase reactions), and patterning by plasma etching is faster.

For dual layer isolation in high frequency devices, plasma oxide has become the preferred material since the oxide has a low dielectric constant and a high breakdown voltage. Plasma oxide is also advantageous for devices that are degraded by hydrogen released from plasma nitride during alloying the top metal layer. Plasma oxide contains only 2-3 at % hydrogen which is firmly bonded to oxygen. To date no parameter shifts have been reported for devices manufactured using the oxide process.

II. PLASMA PROCESSING EQUIPMENT

A. Plasma Etching Equipment

Following the trend in production, plasma equipment manufacturers have introduced production planar plasma etchers. These systems typically have microprocessor control over all system parameters during operation and the cassette handling of 3-in. to 125-mm wafers that semiconductor manufacturers have come to expect in processing equipment. Since dry etching is seldom as selective as wet etching, end point detection schemes, typically based on optical emmission spectra, are included. Additionally some type of substrate cooling system is available to inhibit resist degradation and increase anisotropy.

Often capable of planar plasma etching and RIE, these new systems depart in many cases from traditional wafer batch processing and offer single wafer processing instead. The single wafer processing approach reportedly produces higher yields by better control over etch uniformity. (Contrary to this, dedicated RIE systems generally remain in the batch configuration discussed later.)

In the past single wafer processing has implied lower throughput or higher etching rates which are often undesirable because of possible radiation or photoresist damage. This is no longer the case, because of the larger wafers now in use. The most accurate indication of overall throughput is the total wafer area etched at high yield, not wafers per hour. For example, 750 in.^{2} of wafer area translates to 106 3-in. wafers or 38 5-in. wafers. The larger the wafer, the more competitive single wafer processing is with batch processing (see Figure 30).

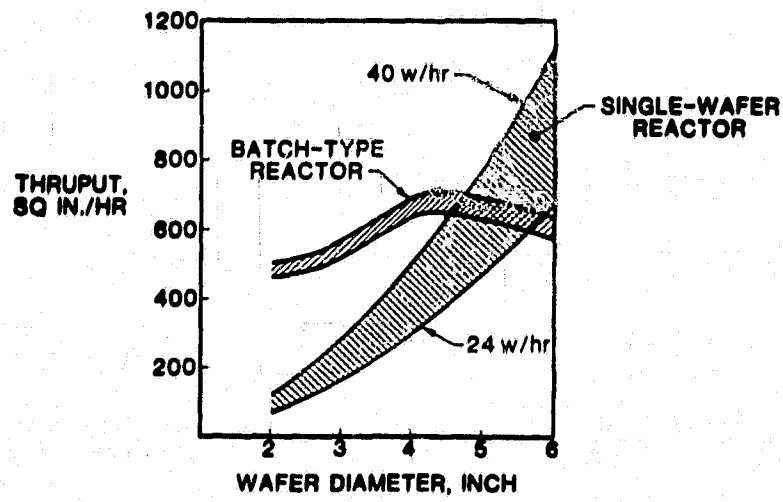


Figure 30. As the wafer size increases to 5- and 6-in. diameters, single wafer processing becomes more competitive with batch processing in terms of total wafer area etched.

Also, as wafer sizes increase, prohibitively large electrodes will have to be used in batch systems to insure uniform plasma throughout the chamber. In turn, the cost and size of the batch systems will increase. Size is important with cost of clean room area estimated at \$200 to \$400/ft^2.

Aware of the advantages of single wafer processing, Lam Research is introducing their Autoetch 480 with single wafer planar plasma etching, throughputs of up to 60 wafers/h and a footprint of 10.5 ft^2. This automatic cassette system is unusual in that it uses a CRT and keyboard in lieu of switches and dials. With the keyboard, an unskilled operator can enter process variables such as flow rates, pressure, RF power, electrode spacing and substrate temperature. During processing, the CRT is placed in a monitor mode and constantly updates all parameters. Dual load-locks reduce particutage contamination on the $165,000 system.

Another single wafer etching system offering keyboard programming and process monitoring is Branson/IPC's Sigma 80. The system's microprocessor directs wafer handling, process control and monitoring. The Sigma 80 uses a walking beam transport system composed of three rails moving in an elliptical pattern to transport wafers through the system. It reportedly produces very low particulate generation from the wafer due to friction. The wafers are transported from a cassette through a load-lock to an inverting wafer chuck. The wafer is held upside down for etching. After etching, the wafer is transported through another load-lock to an output cassette.

The importance of load-locks in plasma etching systems was first realized in initial studies of aluminum etching. Besides eliminating particulates from the ambient atmosphere, load-locks prevent the reaction chamber from absorbing water. In etching aluminum with chlorine gases, the chlorine is absorbed into the photoresist. The Cl ions combine with hydrogen to form HCl which causes a post-etch

on the aluminum. Also, water present in the reaction chamber can form compounds which inhibit etching, producing non-uniformities. However, even with load-locks, the chamber should be cleaned periodically.

One company, Plasma Systems, offers their Plasma Scan option which monitors the composition of the plasma to determine when maintenance is necessary. Their systems detect when the plasma composition varies significantly from the optimum due to particulate build up and institute a cleaning cycle of very reactive plasmas which clean the particulates off the chamber walls and electrodes.

Plasma Systems has just introduced the model 2406. Combining the capabilities of the 2106 and the 2206, the 2406 performs both planar plasma etching and RIE. The system's microprocessor controls all system parameters and can store the values for these parameters for up to 146 process steps. The $135,000 system features cassette handling, dual load-locks and walking beam transport.

Tokyo Ohka claims to have sold over 200 systems in Japan for in-line mass production systems that process wafers one at a time. Although their OAPM systems are cassette-to-cassette, they can be easily interfaced for complete in-line operation. The OAPM-500 is a load-locked planar plasma etching or RIE system which employs a self-cleaning cold-trap. While cold-traps are beneficial to processes absorbing detrimental compounds such as aluminum chloride, many manufacturers are reluctant to use them for safety reasons. In many cases they trap noxious and explosive gases. By automating the cold-trap cleaning, Tokyo Ohka feels that potential safety hazards are eliminated. The OAPM-500's substrate holder can be

heated or cooled for different processes. The holder can also be changed, allowing different holder materials to be used, depending on the gases used in the process.

The gases used for plasma etching are usually either fluorine- or chlorine-based depending on the film to be etched. The different gases make the choice of electrode and chamber materials critical. In their DWE-100, Drytek, for example, uses an electrode assembly of aluminum and Teflon. The DWE-100 is designed for planar plasma etching. The DWE-100 will process from one to six wafers at a time on six independent, vertical electrodes. This allows throughputs (which are always process dependent) to range from 25 to 100 wafers/h. With dual load-locks and an optional laminar flow hood to reduce particulate contamination, the system takes up 9 ft^2 of floor space and stands less than 8 ft high. Base price for the system is under $70,000.

Eaton/D&W uses a multiple/single station configuration to allow single wafer processing at higher throughputs on their model 5000. The load-locked cassette system reportedly achieves production throughputs at conservative etching rates using this configuration. The multiple stations are controlled on a single wafer basis. End point detection is claimed to be unnecessary because of the conservative etching process has high selectivity.

Instead of using multiple stations, Tegal has developed a fast dual step etching process for polysilicon. After the end point is detected etching with fluorine, the etch is made anisotropic using

a chlorine gas to remove residual polysilicon. Developed for their model 700, the process can be used in the newer model 701. Priced at $76,000, the 701 features cassette handling with manual or automatic sequencing, automatic end point detection with delay timer and two process channels for easy process change over. Their model 702 is designed for aluminum etching and preliminary pricing is in the $130,000 range.

LFE's model 8001 is another aluminum etcher. It uses the multireactor configuration. To eliminate post etching caused by absorbed chlorine in the photoresist, the 8001 has an integral photoresist strip station. The photoresist strip station does not slow down throughput of the dual load-locked system since the strip is faster than the aluminum etching cycle. A microcomputer allows single wafer processing through the multiple reactors to end point detection.

Presently offering a batch system, Perkin-Elmer is introducing a single wafer etching system that is dedicated to planar plasma etching. The new system is fully automated to enhance throughput and will accommodate a wide range of fabrication parameters. The system offers pre- and post-processing features such as wafer de-scumming and photoresist strip, and load-locked.

In all fairness, there are some noteworthy batch systems from MRC and ET Equipments that use in-line configurations. MRC's model MH-100 moves wafers along a double "C" shaped track while the wafers are turned on their axes. Each wafer sees the same position every 25 s for maximum uniformity. The plasma averaging technique

gives etching uniformities of ± 3% across the wafer and from wafer to wafer.

ET Equipments' Plasmafab 4200 is an automatic in-line plasma etching system with cassette handling and processing capability of up to 20,000 4-in. wafers/week with ± 3% uniformities. At the heart of this system is ET Equipments' Omega Track wafer handling system. This handling system uses simple belt conveyors under atmosphere where feasible, combined with rotary handling under vacuum. As a result, gears, chains and vibrating tracks are eliminated, which ET Equipments claims have caused reliability problems.

Plasma-Therm manufactures only batch systems for planar plasma etching or RIE. Their modular component construction allows upgrading or change over from one technique to another. Configured in the model PK 2440 PE/RIE, the dual system is attractive due to its ability to operate in plasma etch, RIE or triode etch modes.

B. Plasma Deposition Equipment

Commercial systems have now evolved through many modifications, and Applied Materials' Plasma II plasma nitride reactor is typical of that evolution. Plasma II is a second-generation system built from experience gained through the use of Plasma I, the first commercially available planar plasma reactor. The present Applied Materials system can process 42 3-in. wafers at a time and has an etch-deposit option to pre-clean wafers prior to deposition. In the first quarter of 1980, Applied Materials introduced the Plasma III. This third-generation system produces higher quality films by

reducing the particulate level and increasing the deposition temperature. From the basic planar reactor design of Figure 28, other manufacturers have tried to improve the productivity of silicon nitride reactors. ET Equipments manufacturers the Model 330N and the Model 4200N. The Model 330N is designed to load platens of wafers through a horizontal slot door while the system is maintained at processing temperatures. This loading scheme minimizes the exposure of the electrodes and the inside of the reactor to the atmosphere, an essential for operating a cleaner, higher throughput system. When the interior of a reactor is exposed to the atmosphere and temperature cycling, flaking of the residual film from the inner reactor surfaces becomes a particulate problem. By reducing atmospheric exposure ET Equipments has reduced the need for time-consuming cleaning runs between production runs.

The Model 4200N is an inline machine--a cassette-to-cassette, batch-loading machine capable of depositing 6000 Å of silicon nitride on 70 wafers/h. This machine has been successful in reducing particulates because it uses a vibration-free transport mechanism for moving wafers through a load lock into the deposition chamber and out into unloading cassettes.

In another approach to inline processing, LFE Corporation offers the System 8000. This system is a cassette-to-cassette inline continuous processor which moves the wafers along a track through five sequential deposition chambers. The System 8000 uses a silane/nitrogen-only reaction which the company claims eliminates the hydrogen and oxygen components from the nitride, producing a denser

film with better etching characteristics. The elimination of hydrogen from a silicon nitride film prevents formation of an ammonium fluroride film which, if it forms during silicon nitride etching, inhibits further etching.

Because the System 8000 is never opened to the atmosphere and is always maintained at processing temperatures, LFE has reduced the flaking of silicon-rich nitride which forms on the non-heated electrode of the processing chamber.

Another supplier of silicon nitride deposition equipment is Tegal. Their Model 302 is a side-loading system which uses square electrodes to achieve a greater deposition area and thus higher throughput. Because they are square, the electrodes do not rotate. Uniformity is reportedly controlled by introducing the reactant gases through a perforated upper electrode. Theoriginal PD applications have been for silicon nitride, and system development has concentrated on this needs. Other films that can be plasma deposited include silicon dioxide, silicon oxynitride, aluminum oxide, and amorphous silicon (a-Si).

Potential uses for plasma silicon dioxide, either doped or undoped, are for passivation, intermetallic dielectrics, reflow, masking, or diffusion sources.

At present, planar systems cannot process doped films in a production environment because of the operator's potential harmful exposure to toxic dopants absorbed over the large area of the reactor surface. Plasma deposition of silicon dioxide is the choice when advantage can be taken of low wafer processing temperatures. When

deposited undoped, silicon dioxide presents no danger because the reactants are silane and nitrous oxide.

It appears likely that applications other than silicon nitride might now be considered for production use, or be safe for production use, with the sudden appearance of vertical, longitudinal flow reactors, a system which seems to have overcome many of the shortcomings of the radial flow reactors.

A brain child of inventor George Engle of the George Engle Co. in Phoenix, Arizona, the vertical, longitudinal flow reactor is offered by two manufacturers--Pacific Western Systems, Inc. (PWS) in Mountain View; California, and ASM/America.

A schematic overview of this new reactor system is shown in Figure 31. As in standard LPCVD, the reactor consists of a quartz furnace tube with resistant heating. Gases are introduced at the load/unload end of the tube, and pressure is monitored with a capacitance sensor to control evacuation and system pressure from the opposite end. The reactor's internal configuration consists of graphite slabs electrically isolated from one another by quartz spacers. RF power input is to alternate slabs so that a plasma field can be set up between each slab (see Figure 32). Wafers are then placed in pockets on each side of the slab except on the outside of the end slab. The "boat" of wafers, which is loaded outside the system, is pushed into the furnace tube. Electrical connections to the RF power supply are made through sliding contacts.

By moving the wafers to a vertical processing position both the run size and particulate problems have been improved.

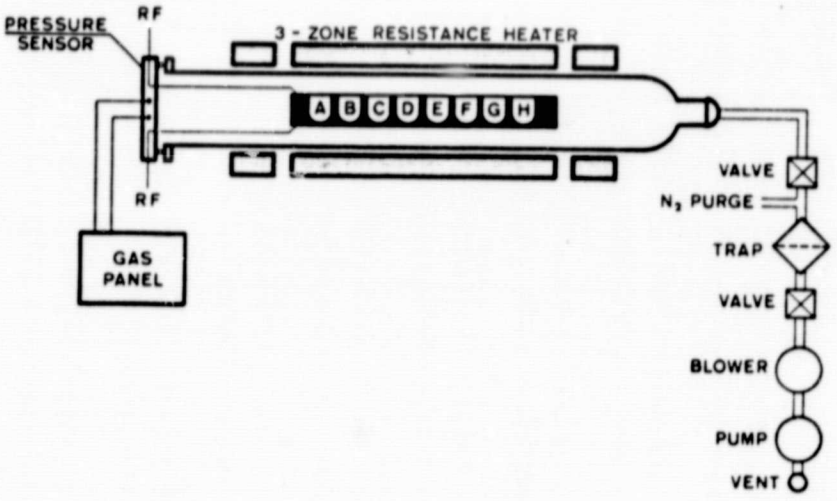


Figure 31. The cross-section of a vertical, longitudinal flow plasma deposition system shows how this design has brought the inherent advantages of vertical wafer processing to plasma enhanced deposition.

The use of graphite electrodes, instead of aluminum, is advantageous in that reportedly this system experiences no flaking of the residual films from the electrodes when they are pulled from the system and cooled.

Another advantage of longitudinal flow reactors is that they can be used to deposit doped films, something not recommended on a radial flow reactor because of possible toxicity problems. The design of the longitudinal reactor is similar to that of a diffusion furnace with a scavenger exhaust system preventing toxic substances from escaping into the atmosphere. Therefore it is believed that these systems will find applications in the deposition of toxic substances such as phosphorus, arsenic, and boron doped silicon dioxides and silicon.

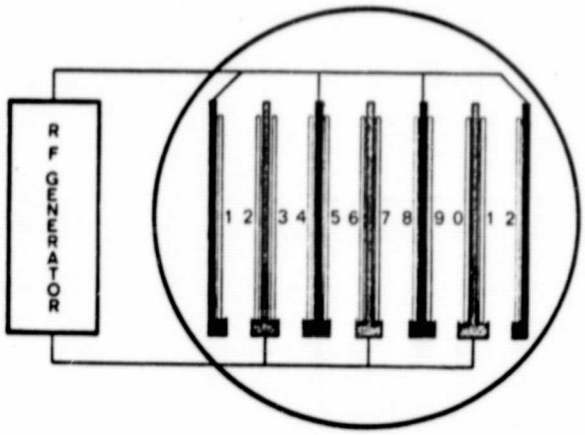


Figure 32. Multi-level vertical electrodes (graphite slabs) enable new plasma deposition systems to increase production throughput and, reportedly, improve film quality.

C. A Survey of Plasma Processing Equipment Vendors and Models

The information presented in Table IX represents some of the more typical vendors of dry processing etching and deposition equipment.

III. PRESENT AND FUTURE TRENDS IN SEMICONDUCTOR TECHNOLOGY

A. Introduction

With continued steady and abundant improvements in the three principal semiconductor processing steps--lithography, etching, and ion implantation--record breaking performance of integrated circuits in the near future is inevidible. Advances in both the processing and the equipment to do the processing coupled with the

TABLE IX - DRY PROCESSING VENDORS AND EQUIPMENT CHARACTERIZATION

COMPANY AND CONTACT PERSON	MODEL OR SERIES NUMBER	TYPE						CHARACTERISTICS									MATERIAL							WAFER SIZE			THROUGH PUT	RF POWER (KW)	RF FREQUENCY (HZ)	GAS FLOW		ELECTRODE MATERIAL	CHAMBER MATERIAL	END PT. DET.		PUMP SYSTEM				SIZE	COST ($\times 10^3$)	OTHER COMMENTS
		PLASMA DEP	RE-BARRELL	RE-PLANAR	RIE	ION MILL	OTHER	MANUAL	AUTO	UP CONTROL	SINGLE	BATCH	LOAD LOCK	CASSETTE TO CASSETTE	TRANSPORT SYSTEM	PRODUCTION R AND D	PR	OXIDE	NITRIDE	POLY SI	Al	Al ALLOY	OTHER	2,3 INCH	4 INCH	5 INCH				MASS FLOW	OTHER			OPTICAL	OTHER	MECHANICAL	CYRO	DIFFUSION	OTHER			
ANELVA Roger Fox 408-744-1780	503			X	X							X				X			X	X	X	X		X	X	X		1	13.56M		X				X	X				S1	100	
	4001			X	X				X	X		X	X	X	TR1	X			X	X	X	X	MP1	X	X	X	TH1	2	13.56M		X	Al	SS		EP 1				PS 1	S2	300	A1
ASM/AMERICA Duane Hoffman 602-243-4221	Single Tube	X								X		X				X			X	X	X			X	X	X	TH2	4	450K	X					X	X				S20	117	A20
	Double Tube	X								X		X				X			X	X	X			X	X	X	TH3	4	450K	X					X	X				S20	207	
BRANSON (DIONEX or I.P.C.) Cory Mullins 415-489-3030	Sigma 80 for poly, oxide			X					X	X	X		X	X	TR2	X			X		X			X	X		TH4	1	13.56M	X		Al	Al			X				S3	150	A2
	Sigma 80 for aluminum			X					X	X	X		X	X	TR2	X			X	X	X	X	MP2	X	X		TH5	1	13.56M	X		Al	Al	X		X				S3	260	A2
COBERLY Ed Hrbacek 408-727-1530	TRIE 303			X	X				X	X	X		X	X	TR9	X			X		X	X		X	X	X	TH6	1	13.56M	X		SS	SS		X	X		X		S14	310	A14
COMMONWEALTH SCIENTIFIC John Tkach 703-548-0800	MILLTRON IV				X	X			X		X	X	X			X		X		X	X	X		X	X	X	TH7		13.56M		X	W	SS or Al	X	EP 3		X	X		S16	100	A16
CVC V.L.Schoonover, Inc 404-396-8877	MOS-601	X						X	X			X			TR16	X			X	X	X	X	X	X	X	X	TH8	5	50K		X	Cu	SS		EP 1	X		X		S31		A32
	601	X						X				X			TR16	X			X	X	X	X	X	X	X	X	TH8	5	50K or 13.56M		X	Cu	SS		EP 1	X	X	X		S31		A32
DRYTEK Art Zafiropoulo 617-657-3933	DRIE 100			X					X	X	X	X		X	TR11	X				X	X		Si,W	X	X	X		1	13.56M	X	X	Al	Al		EP 4	X				S19	75	A19
	DRIE 100-SP			X					Y	X	X	X			TR11		X			X	X		Si,W	X	X	X		1	13.56M	X	X	Al	Al		EP 4	X				S19	71	A19
EATON Art Loc 305-773-1150 Clint Graves 408-727-1190	5000			X					X	X	X		X	X	TR4	X			X	X				X	X	X	TH9	8	100K	X		Al	SS				X			S6	95	A5
	5200			X					X	X	X		X	X	TP4	X			X	X	X			X	X	X	TH9	8	100K	X		Al	SS				X			S6	120	A5
	5500			X					X	X	X		X	X	TR4	X			X	X	X	X		X	X	X	TH9	8	100K	X		Ti Alloy	SS				X		PS 1	S6	140	A5
	425			X					X			X				X	X		X	X	X	X		X	X	X	TH10	9	450K		X	Ti Alloy	SS				X			S7	150	A6
	WAFER GLIDE 85						T1		X	X	X			X	TR5	X			Y	X		X	X	MP3	X	X	X	TH11	5			X								X	S8	250	A7
ET SYSTEMS (ELECTROTECH) 516-231-3700	4200 (metals)			X					X	X		X	X	X	TR3	X					X	X		X	X		TH12		380K	X		Alloy			X		X	X		S4		A3
	4200ND (dielectrics)			X					X	X		X	X	X	TR3	X			X	X				X	X		TH12		380K	X		Alloy			X		X	X		S4		A3
	425			X				X	X			X				X	X		X	X				X	X				380K	X	X				X	X						A4
	330NX	X						X				X				X			X					X	X		TH13		380K		X				X	X				S5		

TABLE IX (Continued)

COMPANY AND CONTACT PERSON	MODEL OR SERIES NUMBER	TYPE						CHARACTERISTICS								MATERIAL							WAFER SIZE			THROUGH-PUT	RF POWER (KW)	RF FREQUENCY (HZ)	GAS FLOW		ELECTRODE MATERIAL	CHAMBER MATERIAL	END PT. DET		PUMP SYSTEM			SIZE	COST ($X10^3$)	OTHER COMMENTS
		PLASMA DEP	PE-BARRELL	PE-PLANAR	RIE	ION MILL	OTHER	MANUAL	AUTO	UP CONTROL	SINGLE	BATCH	LOAD LOCK	CASSETTE TO CASSETTE	TRANSPORT SYSTEM	PRODUCTION	R AND D	PR	OXIDE	SITRIDE	POLY SI	AL	AL ALLOY	OTHER	2.5 INCH	4 INCH	5 INCH				MASS FLOW	OTHER			OPTICAL	OTHER	MECHANICAL	CRYO	DIFFUSION	OTHER			
ET SYSTEMS (Continued)	504B		X					X				X				X		X							X	X		TH14	6	60K			A1	A1		X	X					
	450			X				X				X				X		X	X	X		X	X		X	X		TH15	7	*						X	X					
	MS330						T1	X	X			X					X							MP4	X	X		TH16	10	DC						X	X					A8
	MS4100						T1		X			X	X			X			X	X	X		X		MP4	X	X		TH16	10	DC						X	X					A8
IONIC SYSTEMS Ron Kubacki 408-946-7717	IONIC	X							X	X		X	X		TR10	X				X					X	X	X	TH17	2	13.56M	X		SS	A1		X	X			S15		A15
LAM John Voehl 408-496-6999	580			X					X	X	X		X		TR13	X			X						X	X	X	TH18	.5	13.56M		X			X		X			S22	165	A23
	480			X					X	X	X		X		TR12	X				X	X				X	X	X	TH18	.5	13.56M		X	T1	A1	X		X			S22	165	A23
LFE Mike Bennette 617-365-4511 ext. 1049	8500A			X					X	X	X		X	X	TR15	X					X	X			X	X	X	TH19	1.5	13.56M	X		A1	A1	X		X			S29	180	A29
	8500-D,N	X							X	X	X		X	X	TR15	X			X	X					X	X	X	TH20	1.5	13.56M	X		A1	A1	X		X			S29	150	A31
	1002		X					X	X			X				X		X	X	X	X				X	X	X	TH21	.5	13.56M		X	A1	Qrtz		X	X			S30	55	A31
MICROETCH (VEECO)	10"					X						X				X		X	X		X	X	X	GaAs Mo	X	X		TH22	20	13.56M		X	W			X	X		X	S9	115	A9
	747					X						X					X	X	X		X	X	X	GaAs Mo	X	X		TH22		13.56M		X				X	X		X		50	
	3"-7700					X						X				X		X	X		X	X	X	GaAs Mo	X	X		TH22		13.56M		X				X	X		X	S9	50	A9
MRC Jim Grant 214-234-8273	MH 100						T2	X	X	X		X			TR8	X			X	X	X				X	X		TH23	1.5	50K 13.56M	X		SS	SS		X	X	X		S10	90	A10
	WAFER LINE 80	X							X	X	X		X	X	TR7	X			X	X		X	X			X	X	TH25	1.5	13.56M	X					X		X		S12	300	A12
	603						T1		X	X		X	X		TP8	X			X	X	X			MP6	X	X	X	TP24	1.5	13.56M		X	SS	SS		X		X		S13	180	A13
	900						T1	X	X	X		X	X		TR6	X			X	X	X			MP7	X	X	X	TH24	1.5	13.56M		X	SS	SS		X		X		S11	150	A11
PACIFIC WESTERN Bill Snow 415-961-8855	450 COYOTE	X								X		X				X			X	X	X				X	X	X	TH26	.7	450K		X	Graph	Qrtz				X		S21	100	A21
	450 COYOTE II	X								X		X				X			X	X	X				X	X	X	TH26	.7	450K		X	Graph	Qrtz				X		S21	200	A21
PERKIN/ELMER Keith Mortenson 203-834-4103	OMNIETCH 10,000			X					X	X	X		X	X	TR17	X			X	X	X	X			X	X	X	TH27	.4	13.56M	X				X		X		X		S32	275	A33
	24008 SA 24008 SL	X						X				X					X							MP8	X	X	X			13.56M	X					X		X				130	A34
	4400's						T1	X				X				X			X	X				MP9	X	X	X	TH27	.2	13.56M	X			SS		X		X		X	S33	250	A35

TABLE IX (Continued)

COMPANY AND CONTACT PERSON	MODEL OR SERIES NUMBER	TYPE						CHARACTERISTICS									MATERIAL						WAFER SIZE			THROUGH-PUT	RF POWER (KW)	RF FREQUENCY (HZ)	GAS FLOW		ELECTRODE MATERIAL	CHAMBER MATERIAL	END PT. DET.		PUMP SYSTEM			SIZE	COST ($X10^3$)	OTHER COMMENTS
		PLASMA DEP	PE-BARRELL	PE-PLANAR	RIE	ION MILL	OTHER	MANUAL	AUTO	µP CONTROL	SINGLE	BATCH	LOAD LOCK	CASSETTE TO CASSETTE	TRANSPORT SYSTEM	PRODUCTION	R AND D	PR	OXIDE	NITRIDE	POLY SI	Al	Al ALLOY	OTHER	2,3 INCH	4 INCH	5 INCH				MASS FLOW	OTHER			OPTICAL	OTHER	MECHANICAL	CRYO	DIFFUSION	OTHER			
PLASMA THERM Jerry McMahan 214-669-2246	PLASMATRAC 2406			X	X				X	X	X		X	X	TR2	X			X	X		X	X		X	X	X	TH28	.5	13.56M	X			A1		X	X				S24		
	PK 1241			X	X			X	X	X		X				X			X	X	X	X		Cr	X	X	X	TH29	.5	13.56M	X		A1	A1		X	X		X		S25		
	PK 2440			X	X			X	X	X		X				X			X	X	X	X		Cr	X	X	X	TH30	.3	13.56M	X		A1	A1		X	X		X		S12		A25
	PK 2410			X				X	X	X		X				X			X	X	X	X		Cr	X	X	X	TH30	3	13.56M	X		A1	A1		X	X				S26		
	PK 2420				X			X	X	X		X				X			X	X	X	X		Cr	X	X	X	TH31	3	13.56M	X		A1	A1		X	X				S27		
	PK 1231	X						X	X	X		X				X			X	X					X			TH32	.5	13.56M	X			A1			X				S28		
	PK 2430	X						X	X	X		X				X			X	X					X	X	X	TH32	3	13.56M	X			A1			X				S28		
	PK 1250	X		X	X			X	X	X		X				X				X					X			TH33	.5	13.56M	X		A1	A1		X	X				S28		A25
TECHNICS Jack Weiner 703-971-9200	MIN-TLA	X				X		X				X				X	X		X	X	X	X	X	MPI	X	X	X	TH34				X	SS MO C	SS		EP J		X	X		S1F	300	A18
	PE II-A	X		X				X				X				X			X	X	X				X	X			.5	30K		X	A1	A1		X	X				S3K		
TEGAL Billy Liles 512-835-0082 Ken Davidson 215-433-5300	700-701			X				X			X		X	X	TR13	X				X	X				X	X	X	TH35	.3	13.56M	X		A1	A1	X		X				S23	96	A24
	702			X				X			X		X	X	TR13	X						X	X		X	X	X	TH35	.3	13.56M	X		A1	A1	X		X				S23	130	A24
	703			X				X			X		X	X	TR13	X			X						X	X	X	TH35	.3	13.56M	X		A1	A1	X		X				S23	175	A24

TYPES

T1 Sputterer

T2 Vertical plate etcher

T3 DC-RF/PED
DC/RF Diode/Triode Sputter

T4 DC/RF Magnetron
RF Diode

TRANSPORT SYSTEM

TR1 Belt and moving fork

TR2 Walking beam

TR3 Belt conveyor; omega track; continuous batch

TR4 Patented gas track in vacuum, levitates wafer, gravity flow; ½ inch fall in track level

TR5 Air track with guide rail

TR6 Horizontal plate; single pass in line dep; chain drive

TR7 Vertical plate

TR8 Vertical plate with "C" planetary motion

TR9 "Feeder" system

TR10 Ball bearing slides transport frame into chamber

TR11 Vacuum pick up on back side of wafer

TR12 Conveyor belt onto mechanical arm

TR13 Bernoulli type pick up and belt

TR15 Vibrator

TR16 Rotostrate wafer holder

TR17 Air track

MATERIALS PROCESSED

MP1 21 different mat'l

MP2 Also Cr, Ti, W, Ta, Mo

MP3 AlSi, AlSi/Cu, TiW followed by Al alloy, etc.

MP4 Au, Ag, Cu, Cr

MP5 DC Mag: Ag, Al, Au, Cr, Cu, Ge, Mo, Nb, Os, Pd, Pt, Re, Rh, Si, Ta, Ti, U, W, Zr, Be
RF Dio: Cr, Ni, Cr, Ti, Au, InSn, TiW
RF Mag: SiO_2, Cermet, Cr/SiO_2

MP6 Chrome mask, Ti/W of BJT

MP7 same as MP5

MP8 Dielectrics, metals, silicides

MP9 Al, Al alloys, Pts, TiW, nichrome gold, nit, ox, $CrSi_2$, per malloy, SiC, TiO_2, dielectrics.

MP10 Ion Miller, etch all semi mat'l

THROUGH PUT

TH1 4" wafer of 1 μAl - 50/hr.

TH2 3" wafer - 108/hr.
100 mm - 70/hr.
125 mm - 30/hr.

TH3 Same as TH2 times 2

TH4 Poly - 100/hr., Oxide - 50/hr.

TH5 Al - 50/hr.

TH6 6 wafer in each run, continuous

TH7 1-2 wafer/hr. single
4 wafer/hr. batch
1050 Å/min SiO_2

TH8 64 - 3"/hr.
AlSi 1000 Å/min

TH9 Al - 50/hr. 1μ
Ox - 50/hr. .5μ
Poly - 100/hr. 5000 Å
Nit - 75/hr.

TH10 Al - 75/hr.
Poly - 200/hr.
Ox - 75/hr.
Nit - 100/hr.

TH11 100/hr Al/Cu

TH12 200 - 3 or 4"/hr.
Batch 80/hr.

TH13 30-3"; 15-4"/hr.

TH14 80 - 3"/hr.
50 - 4"/hr.

TH15 Aug. 4000 Å/hr.

TH16 100 - 3"/hr.

TH17 36 - 100 mm wafer
fit on frame

TH18 40-50 wafer/hr.

TH19 35-40 wafer/hr.

TH20 25-30 wafer/hr.

TH21 50 wafer/hr. avg.

TH22 Si 360 Å/min
GaAs 2600
Ox 400
PR 350
Al 550
Mo 400
40/2", 20/3", 11-4"/hr.

TH23 31 - 3" wafer/hr.
20 - 4" wafer/hr.

TH24 36 - 2"/hr., 16-3"/hr.
9 - 4"/hr. (1 μAl)

TH25 Up to 125 wafers/hr.

TH26 Nit - 300 Å/min.
Ox - 400
Poly - 200

TH27 60 wafers/hr. (Al)

THROUGH PUT (Continued)

TH29 Etch Rates in Angstroms Per Min.

MATERIAL	PE Rate	RIE RATE
Al	To 10K	To 5K
Al/Si	To 10K	To 5K
Al/Cu	To 10K	To 5K
Al/Si/Cu	To 10K	To 5K
Poly Si	To 12K	To 4.5K
SiO_2	To 4K	To 1.5K
Si	To 2K	To 1.2K

TH29 (4-3", 8-2")/hr.

TH30 (8 - 5",14 - 4", 28 - 3", 52 - 2")/hr.

MATERIAL	PE RATE	RIE RATE
Si Nit	1-3K	1.5-3.5K
SiO_2	0.4-2K	0.5 - 1.5K
Poly Si	1-3K	1 - 4K
Al	0.5-2K	1 - 2K
Si	0.2-0.6K	0.3 - 0.8K

TH31 poly 2.5K Å/min.
nit 2.0
ox 1.0
Al 1.5
Si 0.5

TH32 Nitride and Oxide at 300 Å/min.

TH33 same as TH30 plus dep Nitride at 300 Å/min.

TH34 up to 100 waf/hr.

TH35 poly, nit 40/hr.
oxide 15-20/hr.
Al 15/hr.

END POINT DETECTORS

EP1 Dual beam monochronometer
EP2 Mass Spec.
EP3 SIM
EP4 Laser Interferometer

PUMP SYSTEM

PS1 Mech (vane or roots) plus liq. N_2

SIZE

S1 503 - 60 x 38 x 73"
pump 40 x 25 x 45"

S2 4001 - 1.7 x 1.05 x 1.5m
pump .8 x 1 x 1.25m
RF 2 x 2 x 4'

S3 3 x 5 x 4'

S4 58 x 48 x 67"

S5 58 x 45 x 49" tabletop

S6 19" x 36" x 53"

S7 57 x 42 x 62"
38 x 36 x 36 pen

SIZE (Continued)

S8 105 x 40 x 72

S9 47 x 33 x 86"

S10 72 x 48 x 61"

S11 70 x 36 x 59"

S12 46 x 30 x 70"
23 x 26 x 60" gen
23 x 26 x 78" instru

S13 78 x 48 x 72"

S14 1.7 x 1.75 x 1.8m

S15 85" x 40"

S16 60 x 30 x 60"
22 x 30 x 72
power supply

S17 17 x 21 x 21"

S18 3 x 4' for 5.5cm
6 x 10' for 35 cm

S19 3 x 3' with
class 10 hood extra

S20 117 x 36 x 76"
48" boat load dock

S21 77 x 38 x 79" (2 tube)
43 (1 tube)

S22 43 x 30 x 46"

S23 all table top
37 x 30 x 23"

S24 67 x 34 x 58"
23 x 26 x 41" gen

S25 46 x 30 x 66"
23 x 26 x 78" gen

S26 46 x 30 x 69"
23 x 26 x 60" gen
23 x 26 x 78 instru

S27 46 x 30 x 70"
23 x 26 x 78 instru
23 x 26 x 60 gen

S28 46 x 30 x 67"
23 x 16 x 78" gen

S29 108 x 35 x 62"

S30 3' x 3' x 3' chamber
3' x 3' x 2' controls

S31 56 x 36 x 42
25 x 25 x 78 control

S32 46 x 40 x 78

S23 64 x 39 x 63 console
23 x 39 x 36 pump
24 x 24 x 44 gen

S34 17½" x 21 x 21

CODE TO TABLE IX (Continued)

ADDITIONAL COMMENTS

A1 - experience
- Japanese

A2 - process research done
- built for prod
- 50 in field
- 17 service centers
- wafer chuck inverts to lessen contamination

A3 - batch capability (12 waf)
- can carry out 4 sequential processes
- over 175 in field
- sold in F or C versions (F or Cl_2)
- maintenance ck on VDU
- RGA to ck vac

A4 - narrow door opening with N_2 purge

A5 - sm. size! includes RF; and pumping; VDU maintenance check, and pumping; up to 6 waf/time
- change over from 3" 4" 5" = $6000
- patented shaped electrode to eliminate "bull's eye" etching (have uniform plasma density over wafer surface
- 2% uniformity
- 425 TTL logic

A6 - 6 Tylan optional
- can convert to PED

A7 - VDU displays pressure
- 4 capabilities; pre heat, pre etch, RF Sputter, ion mill
- 10 KW DC; RF optional for dielectric

A8 - 1-4 magnetrons for sequential layer applications

A9 - Can be used to dep films

A10 - Vertical plate with "C" planetary motion
- Manual overrides micropr
- optimal stop ratio

A11 - Load lock backfills w/inert gas at exchange
- Plates on 2 levels
- use up to 3 targets, mini mag targets available
- radiant substrate heating
- utilization & uniformity, strongest assets

A13 - RF sputter etch, RF diode sputter
- RF & DC mag available
- use up to 3 targets

A14 - can use as either plasma etch or RIE
- most production worthy
- used by Motorola and Zilog

A15 - do not use NH_3 as N source, so have less H_2 problem

A16 - cass to cass in development
- Kaufman type ion source with graphite grids greater etch profile control than plasma
- can be converted to RIE ~ $20,000
- .5 KW DC

A17 - complete pkg
- dual function yet small
- quality construction
- designed and assembled at plan

A18 - load lock not standard but possible
- article in Aug '81 Micro Manufacturing and Testing
- Price given for 35 cm beam size
- Beam sizes: 5.5, 12.5, 20, 35cm
- HP uses for 32 bit with 1u W geom
- Used by: AMI, NCR, HP, IBM, Fairchild, DELCO, Honeywell
- Price increase in May, '82
- Options
  Hood - $25,000
  Mech pump - $7,900
  Blower - $7,900
  Water Recircu - $2,200
  Mass Flow, extra - $2,800
  Chart for Recorder - $980

ADDITIONAL COMMENTS (Continued)

A20 - Throughput can be increased using hi density model to: 160 - 3", 112 - 100 mm, 60 - 125 mm,
- Oil filtration and RF gen on slide out rails for easy maintenance
- vertical wafer orientation

A21 - Oil filtration system
- capacity: 120 - 3", 84 - 4", 36 - 5",
- vertical wafer orientation

A22 - Production RIE will be introduced - June 1982

A23 - Critical etch control

A24 - about 400 in field
- good field service
- 702 uses N_2 load lock, other open

A24 - easy changing from one process to another
- 2440 can also add 2nd gen for biased etching

A24a - designed for continuous production
- preheat prior to etching

A28 - change over requires simple cable relocation

A29 - PR stripping in vacuum
- self cleaning cold trap

A30 - do not use NH_3 for nitride (use SiH_4 (1.75%) + Ar + N_2)
- good stoicheometric Si_3N_4

A31 - More in use than any other machine or market

A32 - excellent step coverage
- 70% layer thickness
- very low radiation damage
- 1 KW sputter etch option
- for cleaning turbo-molecular or cyro pump option

A33 - 32 bit mini computer performs all three: etch, descum, PR strip
- iso and non iso etch
- industry standard gases used
- modular in design
- 4 etchers may run off 1 computer

A34 - static dep
- dynamic dep
  re entrance system

A35 - use up to 3 targets without breaking vac
- chemical etch clean
- can control power to each target
- bias sputter for step
- 3.5 min pump down time
- Delta cathode

intense dedication for developing improved system architectures brighten the prospects for the super-chips of tomorrow.

In lithography, line widths and spacings have reached the 3-μm level on the production line, but 2 μm should occur before 1985. Meanwhile, electron-beam systems are being developed not only for mask generation but also for writing directly on the wafer. And advances in step-and-repeat equipment are proceeding hand-in-hand with advances in projection-alignment equipment. With lines approaching very-fine status, more care must be taken to etch away resists, oxides, or metal from between the lines. Over-etching could occur, and for this reason wet-chemical processes are giving way to dry, nonchemical plasma and reactive ion etching. In addition, other chemicals for resists are being developed, along with new oxide growth and deposition techniques, such as low-pressure chemical-vapor deposition and ion-beam milling. Additional work is progressing in molecular-beam epitaxy, in which the entire epitaxial layer is deposited on the starting wafer one molecular layer at a time for extremely precise control of layer thickness.

To obtain extremely accurate doping profiles, ion implantation is being used by more and more semiconductor manufacturers for the initial impurity deposit; then furnaces are used to drive in the impurities. In fact, some IC manufacturers now use implants to create all of the devices used in high performance circuits. Table X shows some of the changes in processing procedures that wafers are seeing during the transition from LSI to VLSI.

TABLE X

TRENDS IN SILICON WAFER FABRICATION

	LSI	VLSI
Mask Levels	6-8 (1x projection)	10-12 (n x step & repeat)
Minimum feature size (μm)	4-5	1-2
Alignment accuracy (2σ value, μm)	1-2	0.5 or less
Etching technique	Wet (Chemical)	Dry (plasma, ion, etc.)
Process temperature (°C)	900-1200	400-1000
Epi layers	0-1	1-2
Implants	2	4 or more
Interconnects	1-2 (Poly-Si & Al)	3 or more (Silicides, Al-X & others)
Computer-aided manufacturing	No	Necessary
Die size (sq mils)	< 40 k	40-160 k
Yield (%)	10-30	Unknown

Although, E-beam machines are being used by many companies to draw reticles with 1 to 3-μm lines and spaces, relatively few companies in the U.S. use the E-beam machines to draw the patterns directly on the wafer. Typically, the reticles are used with optical-projection equipment to get a final reduction down to the actual chip size (reticles are often generated at ten times the actual chip size).

At any rate, E-beam machines are on the rise. Already, almost every IC manufacturer in Japan uses one either for mask making or for direct writing on the wafer for the critical alignment levels of the layers.

Automation will be a watchword in the development of advanced processing equipment in general. Self-testing features, to make sure settings correspond to actual conditions, will be another key development. Some of the newer systems being installed now offer centralized computer monitoring and control to prevent slip-ups such as trying to process the wafers on the wrong line or accidentally shifting a decimal point on a critical setting.

Many semiconductor manufacturers are now using ion implantation to create the various impurity regions. High-energy ions, when implanted, cause damage to the silicon-crystal lattice structure on the surface of the wafer. To repair this damage, semiconductor manufacturers put the wafers back into the furnaces for several hours to bake and thus anneal the wafer surfaces.

The electron mobility of the annealed material can be increased by using laser-anneal techniques instead of thermal anneal techniques. Unfortunately, laser annealing is a serial process, able to handle one wafer at a time; thermal annealing can handle batches of 40, 50 or more wafers. The benefits of using laser annealing, though, include much better electron mobility in the annealed material, thus leading to higher-speed devices and lower resistance materials. Many companies are experimenting with various forms of laser annealing to improve material and device performance.

Experiments are also underway to anneal polycrystalline material into single-crystal material, paving the way for three-dimensional circuitry.

Although the laser process is slower than thermal annealing, it does eliminate the problems of altered impurity profiles due to extended high temperatures. The laser beam is moved so fast on the surface of the wafer that very little prolonged heat exists. As a result, the diffused impurities remain where they are and the crystal lattice structure easily re-forms.

Another problem looming over the smaller and smaller devices is the high resistance of the thinner and thinner lines that interconnect the devices. Aluminum and polysilicon interconnect lines are starting to show resistances that are too high to permit the low propagation delays possible when devices reach the 1-μm lengths. To counter the problem of high resistance, manufacturers around the world are examining the use of various metal silicides and various refractory metals to serve as the interconnect.

The metal silicides or refractory metals typically offer a tenfold decrease in the resistance when compared to poly or aluminum interconnect.

B. Fine-Line Photolithography

As the density of integrated circuits increases, limits are placed on both the minimum feature size that can be photoprinted and the control which can be achieved in the photoprinting process. Table XI summarizes the characteristics and major limitations of the photoprinting techniques which are presently being investigated by the IC industry.

The table shows that although contact printing is capable of replicating submicron feature sizes, contact printing is unsuitable for VLSI applications because of the defects which are caused on both the photomask and the wafer by the contact process, and because of the runout which is caused by wafer/mask distortion when they are clamped together. For these reasons, even older, less demanding integrated circuit production is being shifted to the contactless proximity and image-projection techniques.

The obvious present contender for submicron lithography is UV exposure. Its dominant advantage is its low cost and high throughput, accented by its established learning curve in optical lithography. Resolution and depth of focus have been significantly improved by the adoption of scanning field projection or direct-step-on-wafer (DSW) exposure. Submicron patterning is possible, with a diffraction-limited resolution of ~0.3 μm.

The new lithographies include proximity x-ray printing and direct writing by either electron beam or ion beam. All three of these technologies have achieved submicron patterns and none are primarily diffraction limited. The resolution capabilities of x rays are primarily limited by practical geometrical considerations, although the fundamental limit for all three technologies is due to primary or secondary electron effects within the resist and substrate layers. Masked systems with flood exposures by electrons or ions have their own practical problems.

All lithographies that use masks with a 1:1 mask/image ratio are also limited by the resolution and accuracy of the masks themselves.

An important subject in submicron technology is registration. As the design rules get narrower, all technologies must pay more and more attention to registration. Registration has a direct influence on circuit density and circuit reliability. The alignment accuracy should typically be about 25% of the feature width. Direct writing or DSW mask systems with registration at each step offer a natural solution to this requirement.

All lithographies are limited either by the exposing machine itself or by diffraction or scattering effects within the resist. The fundamental limitations due to molecular sizes within a polymer resist are on the order of 100 Å. The diffraction limits for UV exposure are ~3000 Å and for x-ray exposure are ~50 -100 Å. The scattering limits, which are dependent on resist thickness for e beams and ion beams, are ~50-800 Å for x-rays, ~200-3000 Å for e beams (with the upper limit set by worst-case conditions for proximity effect backscattering), and ~50-400 Å for ion beams.

For any specified line sizes there are also specifications on the dimensional control of the linewidths and spacings. Typical requirements might be ± 10 to ± 25% of the nominal value. Linewidth accuracy is, to a great extent, controlled by the inherent contrast of the resist, the development process, and the sensitivity to changes in the processing conditions. The resist properties may, therefore, dominate over the inherent lithographic properties in determining the final dimensional accuracy or practical resolution of the final patterns.

TABLE XI

CHARACTERISTICS OF CONTACT AND PROJECTION SYSTEMS

Technique	Minimum Feature Size (μm)	Source Wavelength (Å)	Overlay Tolerance (μm)	Major limitations
Contact	Submicron	Hg	0.5-0.75	Defects, runout, mask cost, line-width variation
Proximity	3-4	Hg Xe	0.5-0.75	Minimum geometry, defects, line-width control
Projection 1:1 1:1 (deep UV)	 2-3 ~0.5	 Hg 2400	 0.5-0.75 ?	 Minimum geometry source, optics, resist availability
Direct step on wafer (DSW)	1.25-1.8	4040	0.125-0.35	Accomodation of wafer distortion
X-ray	~0.3	4-8	?	Source complexity, mask structure, registration
Electron beam direct write on wafer	0.1-0.2	--	0.1-0.3	Cost, throughput

The introduction of linewidths below 0.5 μm into a production mode will require the solution to many problems, not the least of which is the development of high-contrast, reasonably sensitive resists. Dry-processed resists, whose linewidths and profiles are not modified by the swelling and flowing that occur in wet-developed polymer resists, should provide the linewidth control required in a production process. As the resist thicknesses are reduced, more attention will be paid to reduction in defect densities by going to finer filtering for the spin-on resists, or to evaporation, or to plating techniques. Higher-contrast resists will most likely come at the expense of lower sensitivity; this will also delay the introduction of submicron features because of the cost associated with longer exposure times. Poorer sensitivity is, however, a required corollary of finer resolution in order to reduce the statistical probability of exposure-related defects.

The alignment control must be ~ ± 25% of the minimum linewidth. Direct-step-on-wafer techniques for all of the major lithographies offer registration accuracies of ~ ± 0.1 μm. For the near future these registration accuracies should be sufficient. The wafer distortions from process level to process level may, in fact, require DSW lithography for all mask-exposure systems in order to achieve the required alignment within the device patterns. Improvements in alignment accuracy can significantly reduce the total layout area for VLSI chips. For uniform magnification distortion, the mask-to-wafer spacing may be adjusted, without DSW, for exposure from "point" source x rays.

There are also control specifications on focus setting and mask-to-wafer spacing for each of the lithographies. Ultraviolet exposure is severely limited by its narrow depth of focus and will require both automatic alignment and automatic focusing in a LSW mode for submicron definitions. Mask-to-wafer spacing is crucial for x-ray exposure but can be controlled by capacitance sensing techniques. Although there are depth-of-focus limitations for direct writing by e beams or ion beams, they are not particularly restrictive.

Future lithograph will be aided by adoption of the following trends in processing: high-contrast, dry processed resists; more uniform wafer surfaces (e.g., multilevel resist structures); self-aligned device structures; lower temperature processing of device wafers; mix-and-match modes of lithography. Optimum costs may be achieved by using UV exposure for as many levels as possible, x-ray or ion-beam exposure for those levels requiring precise linewidth control, and e-beam exposure for those levels requiring precise alignment. The primary difficulty in such a scheme is to have matched mask sets and matched registration capabilities.

Figure 33 is an attempt to predict the future evolution of production-line lithography for structures with several levels of processing.

The Noyce [90] projections for linewidth reductions have been fairly accurate over the last decade, with production linewidths halving approximately every five years. If this trend is to continue, 1-μm linewidths will not be routinely available before 1985, and 0.5-μm linewidths will not be available before 1990.

It is diffcult to predict whether this trend will be enhanced or retarded. Retarding this trend are the increasing costs of the lithography processing, the resolution limitations of optical/UV exposure, resolution limitations of present resists, linewidth control, and defect density control. Enhancing this trend are the introduction of new processing techniques such as anisotropic, reactive sputter etching, the intensification of development efforts to match the demands of more complex LSI circuits, and the introduction of lithographies with inherently finer resolution capabilities. Direct writing will not be used extensively until the needs for its high sophistication justify its cost; its advent will be shortened by the development of a practical system that will reduce the total writing time by its ability to write both coarse and fine features.

Ultraviolet exposure will continue to be used throughout the 1980s, with bread-and-butter production leveling off at 1.5 to 2.0 μm. Submicron linewidths will not become common on a multiple-level process, production-line basis until at least 1986.

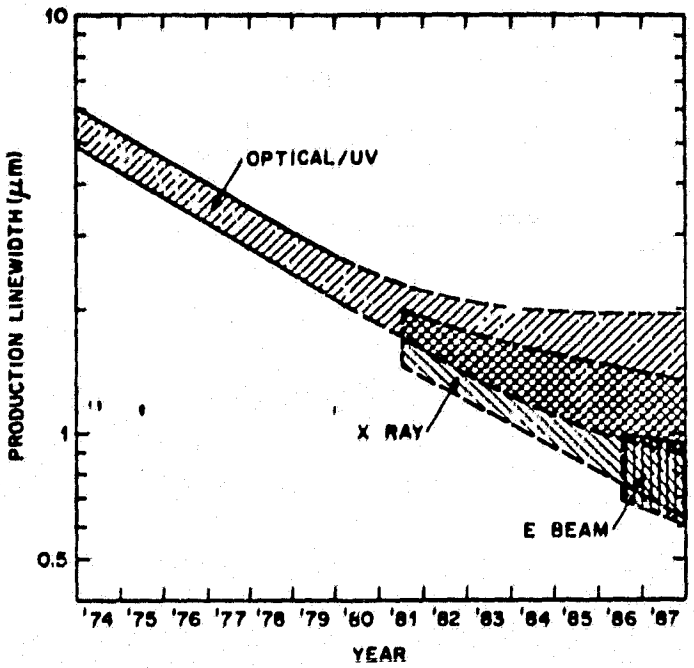


Figure 33. Projections for production linewidths and spacings for optical/UV, x-ray, and e-beam lithographies. The trends shown are for multiple-level production processing.

The first impact of x rays will not be in high-complexity VLSI circuits but rather in lower-complexity circuits for which higher speeds are desired. As yields improve and throughput increases, in the usual "learning curve" fashion, the lower costs with x-ray exposure should allow x rays to supplant many possible UV applications. The acceptance of x rays will depend crucially on alignment capability and more specifically, on the dimensional stability of the mask substrate. The development of a high-resolution, dry-processed resist with a reasonable sensitivity ($<10^{-5}$ C/cm^2) will advance the application of x rays. Ultimately it may still be necessary to go to DSW in order to maintain alignments (and runout). A synchrotron source with multiple

ports may have its cost justified for large-scale production applications.

Electron-beam lithography, as indicated in Figure 33, will not be accepted in a production-line mode until approximately 1986. Currently e beams are being used for some production, but, in those cases where the throughput is reasonable, the linewidths are no better than those that can be resolved by UV, and, in those cases where the linewidths are better than for UV, the throughput is on the order of one 3-4in. wafer/hr. The 1986 date assumes the development of fast-deflection circuitry with 1-nsec spot exposures, sophisticated systems which permit both broad brush aperture exposure of patterns (or their interiors) and fine brush vector exposures of the permeters of selected features, and enhanced software capabilities for proximity corrections. Electron beams should find their first applications in the via window level of integrated circuits. Proximity effect is not a problem for the isolated window features; the window is the most critical level for alignment and for determining layout area, and the total writing area is small enough to guarantee a high throughput. The e-beam registration must be compatible with the UV or x-ray registration for the other levels, but this problem has already been solved on individual systems. For multilevel applications, as implied in Figure 33, e beams will initially find applications in special high-speed circuits and will continue to be used, as the present time, for fast turnaround, low-quantity production.

It is clear that there are several solutions for the realization of submicron lithographies. The pressure for realizing

submicron devices may really be on the controls available in the device processing itself.

C. Low Temperature Processing

A wave of new processing techniques in the arena of additive operations has also surfaced to meet the challenges of VLSI requirements. In general, the trend is "low temperature" for all aspects of additive operations. In the fabrication of VLSI circuits, the temperatures of various operations as well as the sequence of temperature cycles are important to the finished device parameters. For example, movements of doped layers on the order of even a fraction of a μm can significantly influence an MOS device (e.g., source-drain punch-through, voltage, subthreshold leakage current, etc.) with an active channel length of 1-2 μm. The constant drive for more on-chip functional capabilities (e.g., MOS and bipolar devices on the same chip, complementary MOS, complementary bipolar, etc.), keep on adding more thin films and doped layers to a particular structure. Minimization of multi-layer movements through the careful control of temperature sequences is a main concern in fabricating such a structure. To achieve a higher level of integration through lateral as well as vertical down-scaling of structural dimensions can mean extremely stringent controls of process parameters. For example, wafer warpage control is a primary operating temperature can minimize such occurrence. The need for uniform thin gate oxide thickness (200-400 Å) for example, can be better controlled at lower temperatures (slower growth rates). Process induced defects such as oxidation induced stacking faults and wafer slip-line generation due to thermal shock in the furnace also points to the desirability of reducing operating temperatures

during processing. Other special applications of integrated circuits such as operating in radiation environments or detecting and processing of incoming infrared signals, can achieve better hardness or detection sensitivity with lower temperature processing steps as well as correct temperature sequences. Table XII lists potential advantages offered by lowering temperatures of additive operations.

TABLE XII

ADVANTAGES OF LOW TEMPERATURE
ADDITIVE OPERATIONS

1. Minimize lateral as well as vertical movement of doped layers.
2. Better control (e.g., thickness and doping uniformity) for thin layers.
3. Maintains planarity of substrate wafers.
4. Fewer process-induced defects.
5. Enables more processing (thus more functional capabilities per chip) to be incorporated into a particular fabrication sequence with controlled impact on final device characteristics.
6. Improved special device characteristics such as radiation hardness, infrared detectivity, etc.

The low temperature possibility for thermal oxidation is high pressure oxidation. The start of monolithic integrated circuit technology is largely indebted to the discovery and perfection of the ability to grow high quality silicon dioxide at elevated temperature. Traditionally, the oxides are grown in the temperature

range of 900-1200°C at one atmosphere in a furnace tube. The growth rates vary with furnace temperature as well as with ambient conditions (dry oxygen, oxygen and HCI or water vapor). The oxidation duration typically range from 10 minutes up to a few hours for reasons of reproducibility and practicality. Almost every cycle in the IC fabrication requires at least one or more oxidations. The cumulative effects (both temperatures and times) can thus be a significant part of the entire thermal process.

High pressure oxidation can offer the following advantages to VLSI fabrication:

1. Faster oxidation rates at lower temperatures and shorter durations;
2. Reduced cumulative thermal effects on device structure such as junction movement and encroachment;
3. Less thermally-induced damage such as oxidation-induced stacking faults and wafer warpage;
4. Improved Si/SiO_2 interface properties possible because dry oxidation can be used for all oxidation steps;
5. Reduced dopant segregation at Si/SiO_2 interface.

Even though the high pressure oxidation technique enables thick oxides (>1 μm) to be grown in a reasonable time ($\leq$ 2-3 hrs.) and temperature ($\leq$ 1000°C), the oxide thicknesses for VLSI fabrication will probably be about 1 μm or less. For example (see Figure 34) a 5K Å steam-grown oxide can be obtained in about 30 minutes either at 900°C, 10 atm. or at 1150°C, 1 atm. A reduction of 250°C in operating temperature is thus achieved. The reported qualities of high pressure oxides such as oxide density, dielectric

breakdown strength, and fixed oxide charges are either equivalent to or better than those grown at 1 atmosphere. The ability to reduce or suppress the formation of oxidation induced stacking faults with high pressure (6-20 atm.) steam oxidation at relatively low temperatures (700-950°C); the effects of dopant redistribution at the Si/SiO_2 interface are less severe and the radiation hardness of oxide grown at 10 atm. is at least comparable to that of the conventional oxide. All the above point to the emerging of a new low-temperature IC oxidation technique which employs the well-established pressure vessel technology in other industries.

Oxidation is only one example of how low temperature processing may be introduced into the fabrication arena. Table XIII summarized the conventional vs. low temperature possibilities for additive operations in silicon VLSI fabrication.

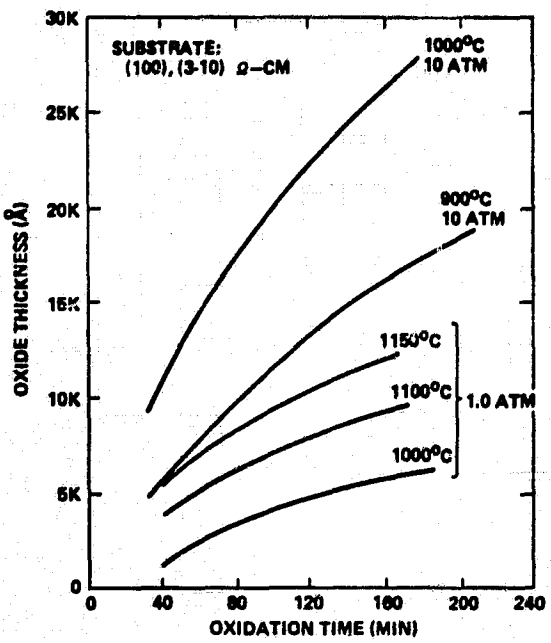


Figure 34. Silicon oxide growth curves under 10 atm. and 1.0 atm. of pressure in a steam ambient.

TABLE XIII

ADDITIVE OPERATIONS AND CONVENTIONAL TECHNIQUES VS. LOW TEMPERATURE (LT) POSSIBILITIES

	OPERATION	CONVENTIONAL TECHNIQUES	LT TECHNIQUES
1.	Thermal Oxidation		
	Gate Oxide	$O_2/H_2O; O_2$ + HCl, T > 900°C	High Pressure Oxidation (700-900)°C
	Isolation Oxide	H_2O, T > 1100°C	High Pressure Oxidation (800-1000)°C
2.	Dopant Incorporation	Thermal Diffusion (900-1200)°C Ion Implantation & Thermal Anneal	Ion Implantation & Beam Annealing
3.	CVD		
	Inter-Level/Passivation Films	Pyrolytic CVD, T $\leq$ 600°C	Plasma-Enhanced CVD (300-400)°C Photo-Excited CVD, $\leq$ 300°C
	Silicon Epitaxy	SiH_4, SiH_2Cl_2, $SiCl_4$ Reactions (1000-1200)°C	Iodine Transport CVD (600-800)°C Solid Phase on Molecular Beam Epitaxy (500-600)°C Vacuum Sublimation $\leq$ 600°C
	Interconnect/Gate Material	Pyrolytic CVD (800-1000)°C	LPCVD (600-800)°C Sputter or E-Beam Deposition (Room Temp. -400°C)

D. Packaging For Dense VLSI Die

Led by mainframe computer manufacturers in the U.S.A. and consumer product manufacturers in Japan, the quest for a ten-times increase in circuit density has spawned some novel packaging approaches.

Virtually every major computer manufacturer is looking at the potential use of chip carriers for their next-generation design where high density is required, particulary in memory hardware. Because of this, there is a growing trend toward an intermediate level of packaging between chip carriers and conventional printed circuit boards, in the form of hybrid modules or multichip substrates. It is quite common to find from two to ten chip carriers mounted on hybrid module. Several of these modules are then assembled onto a conventional PC board, or connected on the edge with a motherboard. At present these interconnection modules are primarily multi-layer ceramic, with the ultimate configuration using multi-layer plastic.

IBM has recently announced a new 23-layer ceramic interconnection module used in its 4331 computer system, which is an astounding achievement for a production ceramic part.

In Japan the emphasis is on gang bonding to achieve high density. Japan's early lead insophisticated consumer packaging utilized LSI devices gang-bonded to plastic substrates in the construction of calculators, watches, and cameras. Recent developments make use of encapsulation systems right on the inner-lead bonding tape.

In Europe, still a different approach to achieving high density has become popular, largely as a result of packaging efforts in the telecommunication industry. Here the use of miniature plastic molded flatpacks (SO packages) has become popular. These small packages, similar to chip carriers with tiny feet, offer the flexibility of rigid surface mounting or through-pole insertion on a PC board with all of the inherent space savings of a chip carrier.

Higher densities achieved at the chip level are creating problems for packaging engineers. As 5μm geometry is pushed through the 3μm level to its near-term goal of 1μm geometry, the increase in electrical field strength between adjacent aluminum traces creates ideal conditions for galvanic corrosion in the presence of moisture. While plasma assisted oxide deposition has reduced the number of defects present in passivation layers, the passivation techniques are still far from perfect, and only one defect is required to set the stage for aluminum corrosion.

On the positive side, operating bias for future memories has been reduced from 17V on many 4K RAMs to 5V on most 16K designs.

Higher voltage fields associated with fine-line geometry not only assist corrosion but also enhance diffusion of ionic contaminating species. Thus, material purity and assemble cleanliness become more critical factors in packaging VLSI devices. One of the most expensive undertakings is a cleanup of the assemble environment. In tackling this problem, Japan has been more aggressive than either the American or European manufacturers. Most Japanese assembly plants are operating at better than Class 10,000 air-

purity conditions, whereas most American and European manufacturers are in the range of Class 20,000 to 100,000 or more.

E. The Role of Integrated Optics

Integrated optics (IO) technology reflects the development of optical subsystems fabricated on a single substrate to perform such functions as generation, detection, control and processing of optical signals. Most research efforts have focused on the development of individual components - modulators, switches, couplers and injection laser sources. But there has been a significant step toward overall integration with the recent demonstration of an IO RF spectrum analyzer by both Hughes and Westinghouse. These devices use a hybrid technology that combines lasers, lithium niobate ($LiNbO_3$) optical waveguides and butt-coupled charged-coupled device (CCD) array detectors, and their specific military significance marks a milestone in the history of integrated optics.

IO devices require materials with specific physical properties (e.g., low transmission loss and large electro-optic coefficient) and materials compatible with fabrication and processing requirements. The three materials generally used for IO components are optical glasses and polymers, $LiNbO_3$ crystals and the III-V semiconductor compounds, notably GaAlAs.

Low-loss channel waveguides can be fabricated in glass by diffusion or ion exchange. Passive glass waveguide components are currently finding their greatest use in combination with optical

fibers as power splitters in both single-mode and multimode applications. One new role for passive waveguides lies in the use of a ring resonator as a sensor, analogous to the sensors that use optical fiber coils. Such an integrated optics ring resonator has been demonstrated in photo-polymerized waveguides by Northrop's Precision Products Division.

$LiNbO_3$ forms the basis for a large number of high-speed electro-optic and acousto-optic switches and modulators. Two-dimensional waveguides can be fabricated by titanium diffusion and coupling between parallel waveguide sections can be electro-optically controlled. Workers in France, Japan and the United States have all demonstrated modulators with GHz response. A Mach-Zender interferometer-type intensity modulator recently reported was fabricated from $LiNbO_3$. It has an 18GHz bandwidth and a power requirement of 11.6μW per MHz.

Because optical fibers tend to depolarize light while $LiNbO_3$ devices generally have a polarization preference, the use of integrated optics components with fibers has required the development of both polarization-independent devices and polarization rotators. Watch for a new generation of IO devices that deals with this polarization problem.

The development of processing techniques for the integration of components will be a continuing major technology challenge for the 1980s. The semiconductor epitaxial growth capabilities have been enhanced greatly by the development of such techniques as metallo-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). These growth techniques improve control

over purity, uniformity and thickness of epitaxial layers in comparison with liquid phase epitaxial growth. The potential for epitaxial growth of GaAlAs layers on high-resistivity GaAs substrates will enable the monolithic integration of a laser with an FET and the fabrication of more sophisticated opto-electronic devices.

IO systems of the 80s will require high-quality semiconductor lasers fabricated with plasma processing technology. The use of such techniques as chemical etching, along with MOCVD and MBE, will enable the definition of lasers and optical and electronic components on the surface of a monolithic chip.

F. VLSI and Technological Innovations

VSLI is a statement about system complexity, not about transistor size or circuit performance. VLSI defines a technology capable of creating systems so complicated that coping with the raw complexity overwhelms all other difficulties. From this definition, we can see that the way in which the industry responds to VLSI must, in fact, be different from the way it has historically evolved through its other phases.

The evolution of the component fields which make up the present VLSI disciplines are shown schematically in Figure 35. Progress in each depends upon those before it being well in place. By now, the number of dramatically new ideas being added to the device physics area is small. Fabrication

technology has essentially all the fundamental knowledge that will be required. Circuit and logic design have some cleverness left but that too will soon saturate. The large system design methodology is still in its exponential phase. Many fundamental ideas have yet to be discovered. The organization and programming of highly concurrent systems are even less well developed. Only a few results are known, and much of the fundamental conceptual apparatus needs to be discovered. A period of very rapid growth lies ahead of us in both of these disciplines. They are central to the difference between VLSI and the current way semiconductor devices are designed. It is here that the major innovative possibilities lie [91].

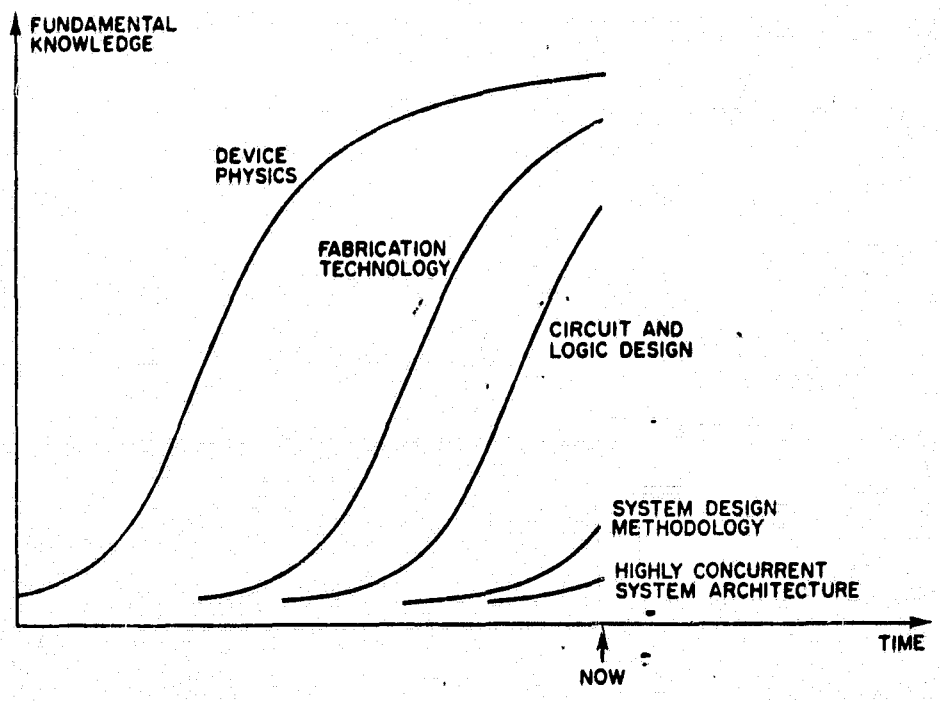


Figure 35. Evolution of VLSI Discipline

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